Description

DRIVE CIRCUIT FOR EL DISPLAY PANEL

Technical Field

The present invention relates to a self-luminous display panel such as an EL display panel which employs organic or inorganic electroluminescent (EL) elements as well as to a drive circuit (IC) for the display panel. Also, it relates to an information display apparatus and the like which employ the EL display panel, a drive method for the EL display panel, and the drive circuit for the EL display panel.

Background Art

Generally, active-matrix display apparatus display images by arranging a large number of pixels in a matrix and controlling the light intensity of each pixel according to a video signal. For example, if liquid crystals are used as an electrochemical substance, the transmittance of each pixel changes according to a voltage written into the pixel. With active-matrix display apparatus which employ an organic electroluminescent (EL) material as an electrochemical substance, emission brightness changes according to current written into pixels.

In a liquid crystal display panel, each pixel works as a shutter, and images are displayed as a backlight is blocked off and revealed by the pixels or shutters. An organic EL display panel is of a self-luminous type in which each pixel has a light-emitting element. Consequently, organic EL display panels have the advantages of being more viewable than liquid crystal display panels, requiring no backlighting, having high response speed, etc.

Brightness of each light-emitting element (pixel) in an organic EL display panel is controlled by an amount of current. That is, organic EL display panels differ greatly from liquid crystal display panels in that light-emitting elements are driven or controlled by current.

A construction of organic EL display panels can be either a simple-matrix type or active-matrix type. It is difficult to implement a large high-resolution display panel of the former type although the former type is simple in structure and inexpensive. The latter type allows a large high-resolution display panel to be implemented, but involves a problem that it is a technically difficult control method and is relatively expensive. Currently, active-matrix type display panels are developed intensively. In the active-matrix type display panel, current flowing through the light-emitting elements provided in each pixel is controlled

by thin-film transistors (transistors) installed in the pixels.

Such an organic EL display panel of an active-matrix type is disclosed in Japanese Patent Laid-Open No. 8-234683. An equivalent circuit for one pixel of the display panel is shown in Figure 62. A pixel 16 consists of an EL element 15 which is a light-emitting element, a first transistor 11a, a second transistor 11b, and a storage capacitance 19. The EL element 15 is an organic electroluminescent (EL) element. According to the present specification, the transistor 11a which supplies (controls) current to the EL element 15 is referred to as a driver transistor 11. A transistor, such as the transistor 11b shown in Figure 62, which operates as a switch is referred to as a switching transistor 11.

The organic EL element 15, in many cases, may be referred to as an OLED (organic light-emitting diode) because of its rectification. In Figure 62 or the like, a diode symbol is used for the EL element 15.

Incidentally, the EL element 15 according to the present specification is not limited to an OLED. It may be of any type as long as its brightness is controlled by the amount of current flowing through the element 15. Examples include an inorganic EL element, a white light-emitting diode consisting of a semiconductor, a typical light-emitting diode, and a light-emitting transistor. Rectification is not

necessarily required of the EL element 15. Bidirectional diodes are also available. The EL element 15 according to the present specification may be any of the above elements.

In the example of Figure 62, a source terminal (S) of the P-channel transistor 11a is designated as Vdd (power supply potential) and a cathode of the EL element 15 is connected to ground potential (Vk). On the other hand, an anode is connected to a drain terminal (D) of the transistor 11b. Besides, a gate terminal of the P-channel transistor 11a is connected to a gate signal line 17a, a source terminal is connected to a source signal line 18, and a drain terminal is connected to the storage capacitance 19 and a gate terminal (G) of the P-channel transistor 11a.

To drive the pixel 16, a video signal which represents brightness information is first applied to the source signal line 18 with the gate signal line 17a selected. Then, the transistor 11a conducts, the storage capacitance 19 is charged or discharged, and gate potential of the transistor 11b matches the potential of the video signal. When the gate signal line 17a is deselected, the transistor 11a is turned off and the transistor 11b is cut off electrically from the source signal line 18. However, the gate potential of the transistor 11a is maintained stably by the storage capacitance (capacitor) 19. Current delivered to the EL element 15 via the transistor 11a depends on gate-source voltage Vgs of the transistor 11a

and the EL element 15 continues to emit light at an intensity which corresponds to the amount of current supplied via the transistor 11a.

Since liquid crystal display panels are not self-luminous devices, there is a problem that they cannot display images without backlighting. Also, there has been a problem that a certain thickness is required to provide a backlight, which makes the display panel thicker. Besides, to display colors on a liquid crystal display panel, color filters must be used. Therefore, there has been a problem of the lowered usability of light. Also, there has been the problem of narrow color reproduction range.

Organic EL display panels are made of low-temperature polysilicon transistor arrays. However, since organic EL elements use current to emit light, there has been a problem that variations in the characteristics of the transistors will cause display irregularities.

The display irregularities can be reduced using current programming of pixels. For current programming, a current-driven driver circuit is required. However, with a current-driven driver circuit, variations will also occur in transistor elements which compose a current output stage. This in turn causes variations in gradation output currents from output terminals, making it impossible to display images properly.

Disclosure of the Invention

To achieve this object, a driver circuit for an EL display panel (EL display apparatus) according to the present invention comprises a plurality of transistors which output unit currents and produces an output current by varying the number of transistors. Also, the driver circuit is characterized by comprising a multi-stage current mirror circuit. A transistor group which delivers signals via voltages is formed densely. Also, signals are delivered between the transistor group and current mirror circuit group via currents. Besides, reference currents are produced by a plurality of transistors.

A first invention of the present invention is a driver circuit for an EL display panel comprising:

reference current generating means of generating a reference current;

a first current source which is fed the reference current from the reference current generating means and outputs a first current which corresponds to the reference current to a plurality of second current sources;

the second current sources which are fed the first current outputted from the first current source and output a second current which corresponds to the first current to a plurality of third current sources; and

the third current sources which are fed the second current

outputted from the second current sources and output a third current which corresponds to the second current to a plurality of fourth current sources,

characterize in that among the fourth current sources, an appropriate number of unit current sources are selected according to input image data.

A second invention of the present invention is a driver circuit for an EL display panel comprising:

a plurality of current generator circuits each of which has unit transistors equal in number to a power of two;

switch circuits connected to the respective current generator circuits;

internal wiring connected to output terminals; and

a control circuit which turns on and off the switch circuits according to input data,

wherein one end of each switch circuit is connected to the current generator circuit and the other end is connected to the internal wiring.

A third invention of the present invention is the driver circuit for an EL display panel according to the second invention of the present invention, wherein:

channel width W of the unit transistors is from 2 to 9 μm both inclusive, and

size (WL) of the transistors is 4 square μm or more.

A fourth invention of the present invention is the driver

circuit for an EL display panel according to the second invention of the present invention, wherein:

a ratio of channel length L to the channel width W of the unit transistors is two or larger; and

power supply voltage used is between 2.5 V and 9 V both inclusive.

A fifth invention of the present invention is a driver circuit for an EL display panel comprising:

a first output current circuit consisting of a plurality of unit transistors which pass a first unit current;

a second output current circuit consisting of a plurality of unit transistors which pass a second unit current; and

an output stage which produces an output by adding an output current of the first output current circuit and an output current of the second output current circuit,

wherein the first unit current is smaller than the second unit current,

the first output current circuit operates in a low gradation region and a high gradation region according to gradations, and

the second output current circuit operates in the high gradation region according to gradations, and output current values of the first output current circuit do not change in the high gradation region when the second output current circuit operates.

A sixth invention of the present invention is a driver circuit for an EL display panel comprising:

a programming current generator circuit which has a plurality of unit transistors corresponding to output terminals;

first transistors which generate a first reference current which defines a current flowing through the unit transistors;

gate wiring connected to gate terminals of the plurality of first transistors; and

a second and third transistors whose gate terminals are connected to the gate wiring and which form current mirror circuits in conjunction with the first transistors,

wherein a second reference current is supplied to the second and third transistors.

A seventh invention of the present invention is the driver circuit for an EL display panel according to the sixth invention of the present invention, comprising:

a programming current generator circuit which has a plurality of unit transistors corresponding to output terminals;

a plurality of first transistors which form current mirror circuits in conjunction with the unit transistors; and

a second transistor which generates a reference current flowing through the first transistors,

wherein the reference current generated by the second transistor branches through the plurality of first transistors.

An eighth invention of the present invention is the driver circuit for an EL display panel according to the sixth or seventh invention of the present invention, wherein in a driver IC chip which includes the driver circuit, the third transistor is electrically connected, in an area in which the first reference current supply wirings are placed, to two outermost placed wirings of the reference current supply wiring group placed in the area.

A ninth invention of the present invention is an EL display apparatus comprising:

a first substrate on which driver transistors are placed in a matrix and which contains a display area consisting of EL elements formed corresponding to the driver transistors;

a source driver IC which applies a programming current or voltage to the driver transistors;

a first wiring formed on the first substrate located under the source driver IC;

a second wiring electrically connected to the first wiring and formed between the source driver IC and the display area; and

anode wiring which branches from the second wiring and applies an anode voltage to pixels in the display area.

A tenth invention of the present invention is the EL display apparatus according to the ninth invention of the present invention, wherein the first wiring has a light shielding function.

An eleventh invention of the present invention is an EL display apparatus comprising:

a display area where pixels with EL elements are formed in a matrix;

driver transistors which supply light-emitting current to the EL elements; and

a source driver circuit which supplies programming current to the driver transistors,

wherein the driver transistors are P-channel transistors, and

transistors which generate the programming current in the source driver circuit are N-channel transistors.

A twelfth invention of the present invention is an EL display apparatus comprising:

a display area where EL elements, driver transistors which supply light-emitting current to the EL elements, first switching elements which form paths between the driver transistors and the EL elements, and second switching elements which form paths between the driver transistors and source signal lines are formed in a matrix;

a first gate driver circuit which performs on/off control

of the first switching elements;

a second gate driver circuit which performs on/off control of the second switching elements;

a source driver circuit which applies video signals to the transistor elements; and

a source driver circuit which supplies programming current to the driver transistors,

wherein the driver transistors are P-channel transistors, and

transistors which generate the programming current in the source driver circuit are N-channel transistors.

A thirteenth invention of the present invention is an EL display apparatus comprising:

EL elements;

P-channel driver transistors which supply light-emitting current to the EL elements;

switching transistors formed between the EL elements and the driver transistors;

a source driver circuit which supplies programming current;

and gate driver circuits which keep the switching transistors off for two horizontal scanning periods or longer in one frame period.

Brief Description of the Drawings

Figure 1 is a block diagram of a pixel in a display panel according to the present invention;

Figure 2 is a block diagram of a pixel in a display panel according to the present invention;

Figure 3 is an explanatory diagram illustrating operation of a display panel according to the present invention;

Figure 4 is an explanatory diagram illustrating operation of a display panel according to the present invention;

Figure 5 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 6 is a block diagram of a display apparatus according to the present invention;

Figure 7 is an explanatory diagram illustrating a manufacturing method of a display panel according to the present invention;

Figure 8 is a block diagram of a display apparatus according to the present invention;

Figure 9 is a block diagram of a display apparatus according to the present invention;

Figure 10 is a sectional view of a display panel according to the present invention;

Figure 11 is a sectional view of a display panel according to the present invention;

Figure 12 is an explanatory diagram illustrating a display panel according to the present invention;

Figure 13 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 14 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 15 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 16 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 17 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 18 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 19 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 20 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 21 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 22 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 23 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 24 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 25 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 26 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 27 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 28 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 29 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 30 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 31 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 32 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 33 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 34 is a block diagram of a display apparatus according to the present invention;

Figure 35 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 36 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 37 is a block diagram of a display apparatus according to the present invention;

Figure 38 is a block diagram of a display apparatus according to the present invention;

Figure 39 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 40 is a block diagram of a display apparatus according to the present invention;

Figure 41 is a block diagram of a display apparatus according to the present invention;

Figure 42 is a block diagram of a pixel in a display panel according to the present invention;

Figure 43 is a block diagram of a pixel in a display panel according to the present invention;

Figure 44 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 45 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 46 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 47 is a block diagram of a pixel in a display panel according to the present invention;

Figure 48 is a block diagram of a display apparatus according to the present invention;

Figure 49 is an explanatory diagram illustrating a drive circuit according to the present invention;

Figure 50 is a block diagram of a pixel in a display panel according to the present invention;

Figure 51 is a diagram of a pixel in a display panel according to the present invention;

Figure 52 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 53 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 54 is a block diagram of a pixel in a display panel according to the present invention;

Figure 55 is an explanatory diagram illustrating a drive method of a display apparatus according to the present invention;

Figure 56 is an explanatory diagram illustrating a drive

method of a display apparatus according to the present invention;

Figure 57 is an explanatory diagram illustrating a cell phone according to the present invention;

Figure 58 is an explanatory diagram illustrating a viewfinder according to the present invention;

Figure 59 is an explanatory diagram illustrating a video camera according to the present invention;

Figure 60 is an explanatory diagram illustrating a digital camera according to the present invention;

Figure 61 is an explanatory diagram illustrating a TV (monitor) according to the present invention;

Figure 62 is a block diagram of a pixel in a conventional display panel;

Figure 63 is a functional block diagram of a driver circuit according to the present invention;

Figure 64 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 65 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 66 is an explanatory diagram illustrating a voltage-based delivery type multi-stage current mirror circuit;

Figure 67 is an explanatory diagram illustrating a current-based delivery type multi-stage current mirror

circuit;

Figure 68 is an explanatory diagram illustrating a driver circuit according to another example of the present invention;

Figure 69 is an explanatory diagram illustrating a driver circuit according to another example of the present invention;

Figure 70 is an explanatory diagram illustrating a driver circuit according to another example of the present invention;

Figure 71 is an explanatory diagram illustrating a driver circuit according to another example of the present invention;

Figure 72 is an explanatory diagram illustrating a conventional driver circuit;

Figure 73 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 74 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 75 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 76 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 77 is an explanatory diagram illustrating a control method of a driver circuit according to the present invention;

Figure 78 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 79 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 80 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 81 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 82 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 83 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 84 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 85 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 86 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 87 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 88 is an explanatory diagram illustrating a drive method according to the present invention;

Figure 89 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 90 is an explanatory diagram illustrating a drive method according to the present invention;

Figure 91 is a block diagram of an EL display apparatus according to the present invention;

Figure 92 is a block diagram of an EL display apparatus

according to the present invention;

Figure 93 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 94 is an explanatory diagram illustrating a driver circuit according to the present invention;

Figure 95 is a block diagram of an EL display apparatus according to the present invention;

Figure 96 is a block diagram of an EL display apparatus according to the present invention;

Figure 97 is a block diagram of an EL display apparatus according to the present invention;

Figure 98 is a block diagram of an EL display apparatus according to the present invention;

Figure 99 is a block diagram of an EL display apparatus according to the present invention;

Figure 100 is a sectional view of an EL display apparatus according to the present invention;

Figure 101 is a sectional view of an EL display apparatus according to the present invention;

Figure 102 is a block diagram of an EL display apparatus according to the present invention;

Figure 103 is a block diagram of an EL display apparatus according to the present invention;

Figure 104 is a block diagram of an EL display apparatus according to the present invention;

Figure 105 is a block diagram of an EL display apparatus according to the present invention;

Figure 106 is a block diagram of an EL display apparatus according to the present invention;

Figure 107 is a block diagram of an EL display apparatus according to the present invention;

Figure 108 is a block diagram of an EL display apparatus according to the present invention;

Figure 109 is a block diagram of an EL display apparatus according to the present invention;

Figure 110 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 111 is a block diagram of a gate driver circuit according to the present invention;

Figure 112 is a timing chart of the gate driver circuit shown in Figure 111;

Figure 113 is a block diagram of part of a gate driver circuit according to the present invention;

Figure 114 is a timing chart of the gate driver circuit shown in Figure 113;

Figure 115 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 116 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present

invention;

Figure 117 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 118 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 119 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 120 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 121 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 122 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 123 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 124 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 125 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 126 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 127 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 128 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 129 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 130 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 131 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 132 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 133 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 134 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 135 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 136 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 137 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 138 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 139 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 140 is an explanatory diagram illustrating a display panel according to the present invention;

Figure 141 is an explanatory diagram illustrating a display panel according to the present invention;

Figure 142 is an explanatory diagram illustrating a display panel according to the present invention;

Figure 143 is an explanatory diagram illustrating a display panel according to the present invention;

Figure 144 is a block diagram of a pixel in a display panel according to the present invention;

Figure 145 is a block diagram of a pixel in a display panel according to the present invention;

Figure 146 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 147 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 148 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 149 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 150 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 151 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 152 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 153 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 154 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 155 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 156 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 157 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 158 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 159 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 160 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 161 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 162 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 163 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 164 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 165 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 166 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 167 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 168 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 169 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 170 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 171 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 172 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 173 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 174 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 175 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present

invention;

Figure 176 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 177 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 178 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 179 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 180 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 181 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 182 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 183 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 184 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 185 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 186 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 187 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 188 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 189 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 190 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 191 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 192 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 193 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present

invention;

Figure 194 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 195 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 196 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 197 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 198 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 199 is an explanatory diagram illustrating a drive circuit of an EL display apparatus according to the present invention;

Figure 200 is an explanatory diagram illustrating a drive method of an EL display apparatus according to the present invention;

Figure 201 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 202 is an explanatory diagram illustrating an EL

display apparatus according to the present invention;

Figure 203 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 204 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 205 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 206 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 207 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 208 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 209 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 210 is an explanatory diagram illustrating an EL display apparatus according to the present invention;

Figure 211 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 212 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 213 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 214 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 215 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 216 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 217 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 218 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 219 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 220 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 221 is an explanatory diagram illustrating a display apparatus according to the present invention;

Figure 222 is an explanatory diagram illustrating a display apparatus according to the present invention;

Figure 223 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 224 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 225 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 226 is an explanatory diagram illustrating a source driver IC according to the present invention;

Figure 227 is an explanatory diagram illustrating a

display apparatus according to the present invention;

Figure 228 is an explanatory diagram illustrating a display apparatus according to the present invention;

(Description of Symbols)

11 Transistor (thin-film transistor)

12 Gate driver IC (circuit)

14 Source driver IC (circuit)

15 EL (element) (light-emitting element)

16 Pixel

17 Gate signal line

18 Source signal line

19 Storage capacitance (additional capacitor, additional capacitance)

50 Display screen

51 Write pixel (row)

52 Non-display pixel (non-display area, non-illuminated area)

53 Display pixel (display area, illuminated area)

61 Shift register

62 Inverter

63 Output buffer

71 Array board (display panel)

72 Laser irradiation range (laser spot)

73 Positioning marker

74 Glass substrate (array board)

81 Control IC (circuit)

82 Power supply IC (circuit)

83 Printed board

84 Flexible board

85 Sealing lid

86 Cathode wiring

87 Anode wiring (Vdd)

88 Data signal line

89 Gate control signal line

101 Bank (rib)

102 Interlayer insulating film

104 Contact connector

105 Pixel electrode

106 Cathode electrode

107 Desiccant

108 $\lambda/4$ plate

109 Polarizing plate

111 Thin encapsulation film

281 Dummy pixel (row)

341 Output stage circuit

371 OR circuit

401 Illumination control line

471 Reverse bias line

472 Gate potential control line

561 Electronic regulator circuit

562 SD (source-drain) short circuit of a transistor

571 Antenna

572 Key

573 Housing

574 Display panel

581 Eye ring

582 Magnifying lens

583 Convex lens

591 Supporting point (pivot point)

592 Taking lens

593 Storage section

594 Switch

601 Body

602 Photographic section

603 Shutter switch

611 Mounting frame

612 Leg

613 Mount

614 Fixed part

631 Current source

632 Current source

633 Current source

641 Switch (on/off means)

634 Current source (single unit)

643   Internal wiring

651   Regulator (current regulating means)

681   Transistor group

691   Resistor (current limiting means,

predetermined-current generating means)

692   Decoder circuit

693   Level shifter circuit

701   Counter (counting means)

702   NOR

703   AND

704   Current output circuit

711   Padder circuit

721   D/A converter

722   Operational amplifier

731   Analog switch (on/off means)

732   Inverter

761   Output pad (output signal terminal)

771   Reference current source

772   Current control circuit

781   Temperature detection circuit

782   Temperature control circuit

931   Cascade current connection line

932   Reference current signal line

941i   Current input terminal

941o   Current output terminal

951   Base anode line (anode voltage line)

952   Anode wiring

953   Connection terminal

961   Connection anode line

962   Common anode line

971   Contact hole

991   Base cathode line

992   Input signal line

1001   Connection resin (conductive resin, anisotropic
conductive resin)

1011   Light absorbing film

1012   Resin bead

1013   Sealing resin

1021   Circuit forming section

1051   Gate voltage line

1091   Power supply circuit (IC)

1092   Power supply IC control signal

1093   Gate driver circuit control signal

1111   Unit gate output circuit

1241   Adjusting transistor

1251   Cutting site

1252   Common terminal

1341   Dummy transistor

1351   Transistor (single-unit transistor)

1352   Sub-transistor

1401   Switching circuit (analog switch)

1491   Flash memory (setting storage means)

1501   Laser device

1502   Laser light

1503   Resistor array (adjustment resistor)

1521   Switch (on/off means)

1531   Steady-state transistor

1541   NAND circuit

1601   Capacitor

1611   Sleep switch (on/off control means, reference current

on/off means)

1671   Protective diode

1731   Coincidence circuit (gradation detection circuit)

1741   Output switching circuit

1742   Changeover switch

1821   Anode connection circuit

2011   Coil (transformer)

2012   Control circuit

2013   Diode

2014   Capacitor

2021   Switch

2022   Temperature sensor

2041   Level shifter circuit

2042   Gate driver control signal

2061   Bonding layer (connection layer, heat conduction layer,

and adhesion layer)

2062   Chassis (Metal chassis)

2063   Projections and depressions

2071   Hole

2211   Control electrode

2212   Video signal circuit

2213   Electron emission protuberance

2214   Holding circuit

2215   On/off control circuit

2221   Selection signal line

2222   On/off signal line

2281   Sealing resin

Best Mode for Carrying Out the Invention

Some parts of drawings herein are omitted and/or enlarged/reduced herein for ease of understanding and/or illustration. For example, in a sectional view of a display panel shown in Figure 11, a thin encapsulation film 111 and the like are shown as being fairly thick. On the other hand, in Figure 10, a sealing lid 85 is shown as being thin. Some parts are omitted. For example, although the display panel according to the present invention requires a phase film such as a circular polarizing plate to prevent reflection, the phase film is omitted in drawings herein. This also applies to the drawings below. Besides, the same or similar forms, materials,

functions, or operations are denoted by the same reference numbers or characters.

Incidentally, what is described with reference to drawings or the like can be combined with other examples or the like even if not noted specifically. For example, a touch panel or the like can be attached to a display panel in Figure 8 to provide an information display apparatus shown in Figures 19 and 59 to 61. Also, a magnifying lens 1582 can be mounted to configure a view finder (see Figure 58) used for a video camera (see Figure 159, etc.) or the like. Also, drive methods described with reference to Figure 4, 15, 18, 21, 23, etc. can be applied to any display apparatus or display panel according to the present invention.

Also, thin-film transistors are cited herein as driver transistors 11 and switching transistors 11, this is not restrictive. Thin-film diodes (TFDs) or ring diodes may be used instead. Also, the present invention is not limited to thin-film elements, and transistors formed on silicon wafers may also be used. In this case, a board 71 can be made of a silicon wafer. Needless to say, FETs, MOS-FETs, MOS transistors, or bipolar transistors may also be used. They are basically, thin-film transistors. It goes without saying that the present invention may also use varistors, thyristors, ring diodes, photodiodes, phototransistors, or PLZT elements. That is, the transistor 11, gate driver circuit 12, and source

driver circuit 14 according to the present invention can use any of the above elements.

An EL panel according to the present invention will be described below with reference to drawings. As shown in Figure 10, an organic EL display panel consists of a glass substrate (array board) 71, transparent electrodes 105 formed as pixel electrodes, at least one organic functional layer (EL layer) 15, and a metal electrode (reflective film) (cathode) 106, which are stacked one on top of another, where the organic functional layer consists of an electron transport layer, light-emitting layer, positive hole transport layer, etc. The organic functional layer (EL layer) 15 emits light when a positive voltage is applied to the anode or transparent electrodes (pixel electrodes) 105 and a negative voltage is applied to the cathode or metal electrode (reflective electrode) 106, i.e., when a direct current is applied between the transparent electrodes 105 and metal electrode 106.

Preferably, the metal electrode 106 is made of metal with a small work function, such as lithium, silver, aluminum, magnesium, indium, copper, or an alloy thereof. In particular, it is preferable to use, for example, an Al-Li alloy. The transparent electrodes 105 may be made of, conductive materials with a large work function such as ITO, or gold and the like. If gold is used as an electrode material, the electrodes become translucent. Incidentally, IZO or other material may be used

instead of ITO. This also applies to other pixel electrodes 105.

Incidentally, a desiccant 107 is placed in a space between the sealing lid 85 and array board 71. This is because the organic EL film 15 is vulnerable to moisture. The desiccant 107 absorbs water penetrating a sealant and thereby prevents deterioration of the organic EL film 15.

Although the sealing lid 85 is used for sealing in Figure 10, the film 111 (this may be a thin film, i.e., a thin encapsulation film) may be used for sealing as shown in Figure 11. The encapsulation film (thin encapsulation film) 111 may be, for example, an electrolytic capacitor film on which DLC (diamond-like carbon) is vapor-deposited. This film features extremely low moisture penetration (high moisture resistance). It is used as the thin encapsulation film 111. Also, it goes without saying that DLC diamond-like carbon) film may be vapor-deposited directly on a surface of the metal electrode 106. Besides, the thin encapsulation film may be formed by laminating thin resin films and metal films.

Desirably, film thickness of the thin film is such that n·d is equal to or less than main emission wavelength λ of the EL element 15 (where n is the refraction factor of the thin film, or the sum of refraction factors if two or more thin films are laminated (n·d of each thin film is calculated); d is the film thickness of the thin film, or the sum of refraction

factors if two or more thin films are laminated). By satisfying this condition, it is possible to more than double the efficiency of light extraction from the EL element 15 compared to when a glass substrate is used for sealing. Also, an alloy, mixture, or laminate of aluminum and silver may be used.

A technique which uses a thin encapsulation film 111 for sealing instead of a sealing lid 85 as described above is called thin film encapsulation. In the case of "underside extraction (see Figure 10; light is extracted in the direction of the arrow in Figure 10)" in which light is extracted from the side of the board 71, thin film encapsulation involves forming an EL film and then forming an aluminum electrode which will serve as a cathode on the EL film. Then, a resin layer is formed as a cushioning layer on the aluminum layer. An organic material such as acrylic or epoxy may be used for a cushioning layer. Suitable film thickness is from 1 μm to 10 μm (both inclusive). More preferably, the film thickness is from 2 μm to 6 μm (both inclusive). The encapsulation film 74 is formed on the cushioning film. Without the cushioning film, structure of the EL film would be deformed by stress, resulting in streaky defects. As described above, the thin encapsulation film 111 may be made, for example, of DLC (diamond-like carbon) or an electrolytic capacitor of a laminar structure (structure consisting of thin dielectric films and aluminum films vapor-deposited alternately).

In the case of "topside extraction (see Figure 11; light is extracted in the direction of the arrow in Figure 11)" in which light is extracted from the side of the EL layer 15, thin film encapsulation involves forming the EL film 15 and then forming an Ag-Mg film 20 angstrom (inclusive) to 300 angstrom thick on the EL film 15 to serve as a cathode (anode). A transparent electrode such as ITO is formed on the film to reduce resistance. Then, a resin layer is formed as a cushioning layer on the electrode film. A thin encapsulation film 111 is formed on the cushioning film.

Half the light produced by the organic EL layer 15 is reflected by the metal electrode 106 and emitted through the array board 71. However, the metal electrode 106 reflects extraneous light, resulting in glare, which lowers display contrast. To deal with this situation, a $\lambda/4$ phase plate 108 and polarizing plate (polarizing film) 109 are placed on the array board 71. These are generally called circular polarizing plates (circular polarizing sheets).

Incidentally, if the pixels are reflective electrodes, the light produced by the organic EL layer 15 is emitted upward. Thus, needless to say, the phase plate 108 and polarizing plate 109 are placed on the side from which light is emitted. Reflective pixels can be obtained by making pixel electrodes 105 from aluminum, chromium, silver, or the like. Also, by providing projections (or projections and depressions) on a

surface of the pixel electrodes 105, it is possible to increase an interface with the organic EL layer 15, and thereby increase the light-emitting area, resulting in improved light-emission efficiency. Incidentally, the reflective film which serves as the cathode 106 (anode 105) is made as a transparent electrode. If reflectance can be reduced to 30% or less, no circular polarizing plate is required. This is because glare is reduced greatly. Light interference is reduced as well.

Preferably, LDD (low doped drain) structure is used for the transistors 11. The EL elements will be described herein taking organic EL elements (known by various abbreviations including OEL, PEL, PLED, OLED) 15 as an example, but this is not restrictive and inorganic EL elements may be used as well.

An organic EL display panel of active-matrix type must satisfy two conditions: that it is capable of selecting a specific pixel and give necessary display information and that it is capable of passing current through the EL element throughout one frame period.

To satisfy the two conditions, in a conventional organic EL pixel configuration shown in Figure 62, a switching transistor is used as a first transistor 11b to select the pixel and a driver transistor is used as a second transistor 11a to supply current to an EL element (EL film) 15.

To display a gradation using this configuration, a voltage corresponding to the gradation must be applied the gate of the driver transistor 11a. Consequently, variations in a turn-on current of the driver transistor 11a appear directly in display.

The turn-on current of a transistor is extremely uniform if the transistor is monocrystalline. However, in the case of a low-temperature polycrystalline transistor formed on an inexpensive glass substrate by low-temperature polysilicon technology at a temperature not higher than 450, its threshold varies in a range of ±0.2 V to 0.5 V. The turn-on current flowing through the driver transistor 11a varies accordingly, causing display irregularities. The irregularities are caused not only by variations in the threshold voltage, but also by mobility of the transistor and thickness of a gate insulating film. Characteristics also change due to degradation of the transistor 11.

This phenomenon is not limited to low-temperature polysilicon technologies, and can occur in transistors formed on semiconductor films grown in solid-phase (CGS) by high-temperature polysilicon technology at a process temperature of 450 degrees (centigrade) or higher. Besides, the phenomenon can occur in organic transistors and amorphous silicon transistors.

As described below, the present invention provides a configuration or scheme which can accommodate the above technologies. Description will be given herein mainly of transistors produced by the low-temperature polysilicon technology.

In a method which displays gradations by the application of voltage as shown in Figure 62, device characteristics must be controlled strictly to obtain a uniform display. However, current low-temperature polycrystalline polysilicon transistors or the like cannot satisfy a specification which prescribes that variations be kept within a predetermined range.

Each pixel structure in an EL display panel according to the present invention comprises at least four transistors 11 and an EL element as shown concretely in Figure 1. Pixel electrodes are configured to overlap with a source signal line. Specifically, the pixel electrodes 105 are formed on an insulating film or planarized acrylic film formed on the source signal line 18 for insulation. A structure in which pixel electrodes overlap with at least part of the source signal line 18 is known as a high aperture (HA) structure. This reduces unnecessary light interference and allows proper light emission.

When the gate signal line (first scanning line) 17a is activated (a turn-on voltage is applied), a current to be passed

through the EL element 15 is delivered from the source driver circuit 14 via the driver transistor 11a and switching transistor 11c of the EL element 15. Also, upon activation of (application of a turn-on voltage to) the gate signal line 17a, the transistor 11b opens to cause a short circuit between gate and drain of the transistor 11a and gate voltage (or drain voltage) of the transistor 11a is stored in a capacitor (storage capacitance, additional capacitance) 19 connected between the gate and drain of the transistor 11a (see Figure 3(a)).

Preferably, the capacitor (storage capacitance) 19 should be from 0.2 pF to 2 pF both inclusive. More preferably, the capacitor (storage capacitance) 19 should be from 0.4 pF to 1.2 pF both inclusive. The capacity of the capacitor 19 is determined taking pixel size into consideration. If the capacity needed for a single pixel is Cs (pF) and an area (rather than an aperture ratio) occupied by the pixel is Sp (square μm), a condition $500/Sp \leq Cs \leq 20000/Sp$, and more preferably a condition $1000/Sp \leq Cs \leq 10000/Sp$ should be satisfied. Since gate capacity of the transistor is small, Q as referred to here is the capacity of the storage capacitance (capacitor) 19 alone.

The gate signal line 17a is deactivated (a turn-off voltage is applied), a gate signal line 17b is activated, and a current path is switched to a path which includes the first transistor 11a, a transistor 11d connected to the EL element 15, and the

EL element 15 to deliver the stored current to the EL element 15 (see Figure 3(b)).

In this circuit, a single pixel contains four transistors 11. The gate of the transistor 11a is connected to the source of the transistor 11b. The gates of the transistors 11b and 11c are connected to the gate signal line 17a. The drain of the transistor 11b is connected to the source of the transistor 11c and source of the transistor 11d. The drain of the transistor 11c is connected to the source signal line 18. The gate of the transistor 11d is connected to the gate signal line 17b and the drain of the transistor 11d is connected to the anode electrode of the EL element 15.

Incidentally, all the transistors in Figure 1 are P-channel transistors. Compared to N-channel transistors, P-channel transistors have more or less lower mobility, but they are preferable because they are more resistant to voltage and degradation. However, the EL element according to the present invention is not limited to P-channel transistors and the present invention may employ N-channel transistors alone. Also, the present invention may employ both N-channel and P-channel transistors.

Optimally, P-channel transistors should be used for all the transistors 11 composing pixels as well as for the built-in gate drivers 12. By composing an array solely of P-channel

transistors, it is possible to reduce the number of masks to 5, resulting in low costs and high yields.

To facilitate understanding of the present invention, the configuration of the EL element according to the present invention will be described below with reference to Figure 3. The EL element according to the present invention is controlled using two timings. The first timing is the one when required current values are stored. Turning on the transistor 11b and transistor 11c with this timing provides an equivalent circuit shown in Figure 3(a). A predetermined current Iw is applied from signal lines. This makes the gate and drain of the transistor 11a connected, allowing the current Iw to flow through the transistor 11a and transistor 11c. Thus, the gate-source voltage of the transistor 11a is such that allows I1 to flow.

The second timing is the one when the transistor 11a and transistor 11c are closed and the transistor 11d is opened. The equivalent circuit available at this time is shown in Figure 3(b). The source-gate voltage of the transistor 11a is maintained. In this case, since the transistor 11a always operates in a saturation region, the current Iw remains constant.

Results of this operation are shown in Figure 5. Specifically, reference numeral 51a in Figure 5(a) denotes a pixel (row) (write pixel row) programmed with current at

a certain time point in a display screen 50. The pixel row 51a is non-illuminated (non-display pixel (row)) as illustrated in Figure 5(b). Other pixels (rows) are display pixels (rows) 53 (current flows through the EL elements 15 of the non-pixels 53 in the display area 53, causing the EL elements 15 to emit light).

In the pixel configuration in Figure 1, the programming current Iw flows through the source signal line 18 during current programming as shown in figure 3(a). The current Iw flows through the transistor 11a and voltage is set (programmed) in the capacitor 19 in such a way as to maintain the current Iw. At this time, the transistor 11d is open (off).

During a period when the current flows through the EL element 15, the transistors 11c and 11b turn off and the transistor 11d turns on as shown in Figure 3(b). Specifically, a turn-off voltage (Vgh) is applied to the gate signal line 17a, turning off the transistors 11b and 11c. On the other hand, a turn-on voltage (Vgl) is applied to the gate signal line 17b, turning on the transistor 11d.

A timing chart is shown in Figure 4. The subscripts in brackets in Figure 4 (e.g., (1)) indicate pixel row numbers. Specifically, a gate signal line 17a(1) denotes a gate signal line 17a in a pixel row (1). Also, *H (where "*" is an arbitrary symbol or numeral and indicates a horizontal scanning line number) in the top row in Figure 4 indicates a horizontal

scanning period. Specifically, 1H is a first horizontal scanning period. Incidentally, the items (1H number, 1-H cycle, order of pixel row numbers, etc.) described above are intended to facilitate explanation and are not intended to be restrictive.

As can be seen from Figure 4, in each selected pixel row (it is assumed that the selection period is 1 H), when a turn-on voltage is applied to the gate signal line 17a, a turn-off voltage is applied to the gate signal line 17b. During this period, no current flows through the EL element 15 (non-illuminated). In non-selected pixel rows, a turn-off voltage is applied to the gate signal line 17a and a turn-on voltage is applied to the gate signal line 17b. During this period, a current flows through the EL element 15 (illuminated).

Incidentally, the gate of the transistor 11a and gate of the transistor 11c are connected to the same gate signal line 11a. However, the gate of the transistor 11a and gate of the transistor 11c may be connected to different gate signal lines 11 (see Figure 32). Then, one pixel will have three gate signal lines (two in the configuration in Figure 1). By controlling ON/OFF timing of the gate of the transistor 11b and ON/OFF timing of the gate of the transistor 11c separately, it is possible to further reduce variations in the current

value of the EL element 15 due to variations in the transistor 11a.

By sharing the gate signal line 17a and gate signal line 17b and using different conductivity types (N-channel and P-channel) for the transistors 11c and 11d, it is possible to simplify the drive circuit and improve the aperture ratio of pixels.

With this configuration, a write paths from signal lines are turned off according to operation timing of the present invention That is, when a predetermined current is stored, an accurate current value is not stored in a capacitance (capacitor) between the source (S) and gate (G) of the transistor 11a if a current path is branched. By using different conductivity types for the transistors 11c and 11d and controlling their thresholds, it is possible to ensure that when scanning lines are switched, the transistor 11d is turned on after the transistor 11c is turned off.

In that case, however, since the thresholds of the transistors must be controlled accurately, it is necessary to pay attention to processes. The circuit described above can be implemented using four transistors at the minimum, but even if more than four transistors including a transistor 11e are cascaded for more accurate timing control or for reduction of mirror effect (described later), the principle of operation is the same. By adding the transistor 11e, it is possible

to deliver programming current to the EL element 15 more precisely via the transistor 11c.

Incidentally, the pixel configuration according to the present invention is not limited to those shown in Figures 1 and 2. For example, pixels may be configured as shown in Figure 140. Figure 140 lacks the transistor 11d unlike the configuration in Figure 1. Instead, a changeover switch 1401 is formed or placed. The switch 11d in Figure 1 functions to turn on and off (pass and shut off) the current delivered from the driver transistor 11a to the EL element 15. As also described in subsequent examples, the on/off control function of the transistor 11d constitutes an important part of the present invention. The configuration in Figure 140 achieves the on/off function without using the transistor 11d.

In Figure 140, a terminal a of the changeover switch 1401 is connected to anode voltage Vdd. Incidentally, the voltage applied to the terminal a is not limited to the anode voltage Vdd. It may be any voltage that can turn off the current flowing through the EL element 15.

A terminal b of the changeover switch 1401 is connected to cathode voltage (indicated as ground in Figure 140). Incidentally, the voltage applied to the terminal b is not limited to the cathode voltage. It may be any voltage that can turn on the current flowing through the EL element 15.

A terminal c of the changeover switch 1401 is connected with a cathode terminal of the EL element 15. Incidentally, the changeover switch 1401 may be of any type as long as it has a capability to turn on and off the current flowing through the EL element 15. Thus, its installation location is not limited to the one shown in Figure 140 and the switch may be located anywhere on the path through which current is delivered to the EL element 15. Also, the switch is not limited by its functionality as long as the switch can turn on and off the current flowing through the EL element 15. In short, the present invention can have any pixel configuration as long as switching means capable of turning on and off the current flowing through the EL element 15 is installed on the current path for the EL element 15.

Also, the term "off" here does not mean a state in which no current flows, but it means a state in which the current flowing through the EL element 15 is reduced to below normal. The items mentioned above also apply to other configurations of the present invention.

The changeover switch 1401 will require no explanation because it can be implemented easily by a combination of P-channel and N-channel transistors. For example, it can be implemented by two circuits of analog switches. Of course, the changeover switch 1401 can be constructed of only P-channel

or N-channel transistors because it only turns off the current flowing through the EL element 15.

When the changeover switch 1401 is connected to the terminal a, the Vdd voltage is applied to the cathode terminal of the EL element 15. Thus, current does not flow through the EL element 15 regardless of the voltage state of voltage held by the gate terminal G of the driver transistor 11a. Consequently, the EL element 15 is non-illuminated.

When the changeover switch 1401 is connected to the terminal b, the GND voltage is applied to the cathode terminal of the EL element 15. Thus, current flows through the EL element 15 according to the state of voltage held by the gate terminal G of the driver transistor 11a. Consequently, the EL element 15 is illuminated.

Thus, in the pixel configuration shown in Figure 140, no switching transistor 11d is formed between the driver transistor 11a and the EL element 15. However, it is possible to control the illumination of the EL element 15 by controlling the changeover switch 1401.

In the pixel configurations shown in Figures 1, 2, etc., one pixel contains one driver transistor 11a. However, the present invention is not limited to this and one pixel may contain two or more driver transistors 11a. An example is shown in Figure 144, where one pixel contains two driver transistors 11a1 and 11a2, whose gate terminals are connected

to a common capacitor 19. By using a plurality of driver transistors 11a, it is possible to reduce variations in programming current. The other part of the configuration is the same as those shown in Figure 1 and the like, and thus description thereof will be omitted.

In Figures 1 and 2, the current outputted by the driver transistor 11a is passed through the EL element 15 and turned on and off by the switching transistor 11d formed between the driver transistor 11a and the EL element 15. However, the present invention is not limited to this. For example, another configuration is illustrated in Figure 145.

In the example shown in Figure 145, the current delivered to the EL element 15 is controlled by the driver transistor 11a. The current flowing through the EL element 15 is turned on and off by the transistor 11d placed between the Vdd terminal and EL element 15. Thus, according to the present invention, the transistor 11d may be placed anywhere as long as it can control the current flowing through the EL element 15.

Variations in the characteristics of the transistor 11a are correlated to the transistor size. To reduce the variations in the characteristics, preferably the channel length of the first transistor 11a is from 5 μm to 100 μm (both inclusive). More preferably, it is from 10 μm to 50 μm (both inclusive). This is probably because a long channel length

L increases grain boundaries contained in the channel, reducing electric fields, and thereby suppressing kink effect.

Thus, according to the present invention, circuit means which controls the current flowing through the EL element 15 is constructed, formed, or placed on the path along which current flows into the EL element 15 and the path along which current flows out of the EL element 15 (i.e., the current path for the EL element 15).

Incidentally, the configuration for use to control the path along which current flows into the EL element 15 is not limited to the pixel configuration in current-programming mode shown in Figure 1, 140, or the like. For example, the pixel configuration in voltage-programming mode shown in Figure 141 can also be used. In Figure 141, placement of the transistor 11d between the EL element 15 and driver transistor 11a makes it possible to control the current flowing through the EL element 15. Of course, the switching circuit 1401 may be placed as shown in Figure 140.

Further, even in the case of current mirroring, a type of current programming, by forming or placing a transistor 11g as a switching element between the driver transistor 11b and EL element 15 as shown in Figure 142, it is possible to turn on and off (control) the current flowing through the EL element 15. Of course, the transistor 11g may be substituted with the changeover switch 1401 in Figure 140.

Incidentally, although the switching transistors 11d and 11c in Figure 142 are connected to a single gate signal line 17a, the switching transistor 11c may be controlled by a gate signal line 17a1 and the switching transistor 11d may be controlled by a gate signal line 17a2 as shown in Figure 143. The configuration in Figure 143 makes pixel 16 control more versatile.

As shown in Figure 42(a), the transistors 11b and 11c may be N-channel transistors. Also, as shown in Figure 42(b), the transistors 11c and 11d may be P-channel transistors.

An object of the present invention is to propose a circuit configuration in which variations in transistor characteristics do not affect display. Four or more transistors are required for that. When determining circuit constants using transistor characteristics, it is difficult to determine appropriate circuit constants unless the characteristics of the four transistors are not consistent. Both thresholds of transistor characteristics and mobility of the transistors vary depending on whether the channel direction is horizontal or vertical with respect to the longitudinal axis of laser irradiation. Incidentally, variations are more of the same in both cases. However, the mobility and average threshold vary between the horizontal direction and vertical direction. Thus, it is desirable that all the transistors in a pixel have the same channel direction.

Also, if the capacitance value of the storage capacitance 19 is Cs and the turn-off current value of the second transistor 11b is Ioff, preferably the following equation is satisfied.

3 < Cs/Ioff < 24

More preferably the following equation is satisfied.

6 < Cs/Ioff < 18

By setting the turn-off current of the transistor 11b to 5 pA or less, it is possible to reduce changes in the current flowing through the EL to 2% or less. This is because when leakage current increases, electric charges stored between the gate and source (across the capacitor) cannot be held for one field with no voltage applied. Thus, the larger the storage capacity of the capacitor 19, the larger the permissible amount of the turn-off current. By satisfying the above equation, it is possible to reduce fluctuations in current values between adjacent pixels to 2% or less.

Also, preferably transistors composing an active matrix are p-channel polysilicon thin-film transistors and the transistor 11b is a dual-gate or multi-gate transistor. As high an ON/OFF ratio as possible is required of the transistor 11b, which acts as a source-drain switch for the transistor 11a. By using a dual-gate or multi-gate structure for the transistor 11b, it is possible to achieve a high ON/OFF ratio.

The semiconductor films composing the transistors 11 in the pixel 16 are generally formed by laser annealing in

low-temperature polysilicon technology. Variations in laser annealing conditions result in variations in transistor 11 characteristics. However, if the characteristics of the transistors 11 in the pixel 16 are consistent, it is possible to drive the pixel using current programming such as the one shown in Figure 1 so that a predetermined current will flow through the EL element 15. This is an advantage lacked by voltage programming. Preferably the laser used is an excimer laser.

Incidentally, the semiconductor film formation according to the present invention is not limited to the laser annealing method. The present invention may also use a heat annealing method and a method which involves solid-phase (CGS) growth. Besides, the present invention is not limited to the low-temperature polysilicon technology and may use high-temperature polysilicon technology.

To deal with this problem, the present invention moves a laser spot (laser irradiation range) 72 in parallel to the source signal line 18 as shown in Figure 7. Also, the laser spot 72 is moved in such a way as to align with one pixel row. Of course, the number of pixel rows is not limited to one. For example, laser may be shot by treating RGB in Figure 72 (three pixel columns in this case) as a single pixel 16. Also, laser may be directed at two or more pixels at a time. Needless

to say, moving laser irradiation ranges may overlap (it is usual for moving laser irradiation ranges to overlap).

Pixels are constructed in such a way that three pixels of RGB will form a square shape. Thus, each of the R, G, B pixels has oblong shape. Consequently, by performing annealing using an oblong laser spot 72, it is possible to eliminate variations in the characteristics of the transistors 11 within each pixel. Also, the characteristics (mobility, Vt, S value, etc.) of the transistors 11 connected to the same source signal line 18 can be made uniform (i.e., although the transistors 11 connected to adjacent source signal lines 18 may differ in characteristics, the characteristics of the transistors 11 connected to the same source signal line can be made almost equal).

In the configuration shown in Figure 7, three panels are placed lengthwise within the length of the laser spot 72. An annealing apparatus which emits the laser spot 72 recognizes positioning markers 73a and 73b on a glass substrate 74 (automatic positioning based on pattern recognition) and moves the laser spot 72. The positioning markers 73 are recognized by a pattern recognition apparatus. The annealing apparatus (not shown) recognizes the positioning markers 73 and determines the location of the pixel column (makes the laser irradiation range 72 parallel to the source signal line 18).

It emits the laser spot 72 in such a way as to overlap with the location of each pixel column for sequential annealing.

Preferably, the laser annealing method (which involves emitting a linear laser spot in parallel to the source signal line 18) described with reference to Figure 7 is used for current programming of an organic EL display panel, in particular. This is because the transistors 11 placed in the direction parallel to the source signal line have the same characteristics (the characteristics of the pixel transistors adjacent in the longitudinal direction are quite similar to each other). This reduces changes in the voltage level of the source signal lines when the pixels are driven by current, and thus reduces the chances of insufficient write current.

For example, in the case of white raster display, since almost the same current is passed through the transistors 11a in adjacent pixels, the current outputted from the source driver IC 14 does not have significant amplitude changes. If the transistors 11a in Figure 1 have the same characteristics and the currents used for current programming of pixels have the same value within the pixel column, the potential of the source signal line 18 during the current programming is constant. Thus, no potential fluctuation occurs in the source signal line 18. If the transistors 11a connected to the same source signal line 18 have almost the same characteristics, there should be no significant potential fluctuation in the

source signal line 18. This is also true to other current-programmable pixel configurations such as the one shown in Figure 38 (thus, it is preferable to use the manufacturing method shown in Figure 7).

A method which involves programming two or more pixel rows simultaneously and which are described with reference to Figures, 27, 30, etc. can achieve a uniform image display (because the method is not prone to display irregularities due mainly to variations in transistor characteristics). In the case of Figure 27, etc., since a plurality of pixel rows are selected simultaneously, if the transistors in adjacent pixel rows are uniform, irregularities in the characteristics of the transistors placed in the lengthwise direction can be absorbed by the source driver circuit 14.

Incidentally, although an IC chip is illustrated in Figure 7 as being stacked on the source driver circuit 14, this is not restrictive and it goes without saying that the source driver circuit 14 may be formed in the same process as the pixel 16.

The present invention, in particular, ensures that a voltage threshold Vth2 of the driver transistor 11b will not fall below a voltage threshold Vth1 of the corresponding driver transistor 11a in the pixel. For example, gate length L2 of the transistor 11b is made longer than gate length L1 of the transistor 11a so that Vth2 will not fall below Vth1 even if

process parameters of these thin-film transistors change. This makes it possible to suppress subtle current leakage.

Incidentally, the items mentioned above also apply to pixel configuration of a current mirror shown in Figure 38. The pixel in Figure 38 consists of a driver transistor 11a through which a signal current flows, a driver transistor 11b which controls drive current flowing through a light-emitting element such as an EL element 15, a transistor 11c which connects or disconnects a pixel circuit and data line "data" by controlling a gate signal line 17a1, a switching transistor 11d which shorts the gate and drain of the transistor 11a during a write period by controlling a gate signal line 17a2, a capacitance C19 which holds gate-source voltage of the transistor 11a after application of voltage, the EL element 15 serving as a light-emitting element, etc.

In Figure 38, the transistors 11c and 11d are N-channel transistors and other transistors are P-channel transistors, but this is only exemplary and are not restrictive. A capacitance Cs has its one end connected to the gate of the transistor 11a, and the other end to Vdd (power supply potential), but it may be connected to any fixed potential instead of Vdd. The cathode (negative pole) of the EL element 15 is connected to the ground potential.

Next, the EL display panel or EL display apparatus of the present invention will be described. Figure 6 is an

explanatory diagram which mainly illustrates a circuit of the EL display apparatus. Pixels 16 are arranged or formed in a matrix. Each pixel 16 is connected with a source driver circuit 14 which outputs current for use in current programming of the pixel. In an output stage of the source driver circuit 14 are current mirror circuits (described later) corresponding to the bit count of a video signal. For example, if 64 gradations are used, 63 current mirror circuits are formed on respective source signal lines so as to apply desired current to the source signal lines 18 when an appropriate number of current mirror circuits is selected (see Figure 64).

Incidentally, the minimum output current of one current mirror circuit is from 10 nA to 50 nA (both inclusive). Preferably, the minimum output current of the current mirror circuit should be from 15 nA to 35 nA (both inclusive) to secure accuracy of the transistors composing the current mirror circuit in the source driver IC 14.

Besides, a precharge or discharge circuit is incorporated to charge or discharge the source signal line 18 forcibly. Preferably, voltage (current) output values of the precharge or discharge circuit which charges or discharges the source signal line 18 forcibly can be set separately for R, G, and B. This is because the thresholds of the EL element 15 differ among R, G, and B (regarding the precharge circuit refer to Figures 70 and 173 and its explanation).

Organic EL elements are known to have heavy temperature dependence (temperature characteristics). To adjust changes in emission brightness caused by the temperature characteristics, reference current is adjusted (varied) in an analog fashion by adding nonlinear elements such as thermistors or posistors to the current mirror circuits to vary output current and adjusting the changes due to the temperature characteristics with the thermistors or the like.

According to the present invention, the source driver 14 is made of a semiconductor silicon chip and connected with a terminal on the source signal line 18 of the board 71 by glass-on-chip (COG) technology. The source driver 14 can be mounted not only by the COG technology. It is also possible to mount the source driver circuit 14 by chip-on-film (COF) technology and connect it to the signal lines of the display panel. Regarding the driver IC, it may be made of three chips by constructing a power supply IC 82 separately.

Panel is tested before the source driver IC 14 is mounted. The test is conducted by applying a constant current to the source signal lines 18.
The constant current is applied by attaching lead wires 2271 to the pads 1522 formed on the ends of the source signal lines 18 and forming test pads 2272 on their ends as illustrated in Figure 227.
By forming the test pads 2272, it is possible to conduct the

test without using the pads 1522.

After the source driver IC 14 is mounted on the substrate 71, its periphery is sealed with sealing resin 2281 as illustrated in Figure 228.

On the other hand, the gate driver circuit 12 is formed by low-temperature polysilicon technology. That is, it is formed in the same process as the transistors in pixels. This is because the gate driver 12 has a simpler internal structure and lower operating frequency than the source driver circuit 14. Thus, it can be formed easily even by low-temperature polysilicon technology and allows bezel width to be reduced. Of course, it is possible to construct the gate driver circuit 12 from a silicon chip and mount it on the board 71 using the COG technology. Also, switching elements such as pixel transistors as well as gate drivers may be formed by high-temperature polysilicon technology or may be formed of an organic material (organic transistors).

The gate driver 12 incorporates a shift register circuit 61a for a gate signal line 17a and a shift register circuit 61b for a gate signal line 17b. The shift register circuits 61 are controlled by positive-phase and negative-phase clock signals (CLKxP and CLKxN) and a start pulse (STx) (see Figure 6). Besides, it is preferable to add an enable (ENABL) signal which controls output and non-output from the gate signal line and an up-down (UPDWN) signal which turns a shift direction

upside down. Also, it is preferable to install an output terminal to ensure that the start pulse is shifted by the shift register and is outputted. Incidentally, shift timings of the shift registers are controlled by a control signal from a control IC 81(see Figures 8 and 208). Also, the gate driver circuit 12 incorporates a level shift circuit which level-shifts external data.

Since the shift register circuits 61 have small buffer capacity, they cannot drive the gate signal lines 17 directly. Therefore, at least two or more inverter circuits 62 are formed between each shift register circuit 61 and an output gate 63 which drives the gate signal line 17(see Figure 204).

The same applies to cases in which the source driver 14 is formed on the board 71 by polysilicon technology such as low-temperature polysilicon technology. A plurality of inverter circuits are formed between an analog switching gate such as a transfer gate which drives the source signal line 18 and the shift register of the source driver circuit 14. The following matters (shift register output and output stages which drive signal lines (inverter circuits placed between output stages such as output gates or transfer gates) are common to the gate driver circuit and source driver circuit.

For example, although the output from the source driver 14 is shown in Figure 6 as being connected directly to the source signal line 18, actually the output from the shift

register of the source driver is connected with multiple stages of inverter circuits, and the inverter outputs are connected to analog switching gates such as transfer gates.

The inverter circuit 62 consists of a P-channel MOS transistor and N-channel MOS transistor. As described earlier, the shift register circuit 61 of the gate driver circuit 12 has its output end connected with multiple stages of inverter circuits 62 and the final output is connected to the output gate 63. Incidentally, the inverter circuit 62 may be composed solely of P-channel MOS transistors. In that case, however, the circuit may be configured simply as a gate circuit rather than an inverter.

Figure 8 is a block diagram of signal and voltage supplies on a display apparatus according to the present invention or a block diagram of the display apparatus. Signals (power supply wiring, data wiring, etc.) are supplied from the control IC 81 to a source driver circuit 14a via a flexible board 84.

In Figure 8, a control signal for the gate driver 12 is generated by the control IC, level-shifted by the source driver 14, and applied to the gate driver 12. Since drive voltage of the source driver 14 is 4 to 8 (V), the control signal with an amplitude of 3.3 (V) outputted from the control IC 81 can be converted into a signal with an amplitude of 5 (V) which can be received by the gate driver 12.

In Figure 8 and the like, what is denoted by reference numeral 14 has been described as a source driver, but instead of being a mere driver, it may incorporate a power circuit, buffer circuit (including a circuit such as a shift register), data conversion circuit, latch circuit, command decoder, shifting circuit, address conversion circuit, image memory, etc. Needless to say, a three-side free configuration or other configuration, drive system, etc. described with reference to Figure 9 and the like are also applicable to the configuration described with reference to Figure 8 and the like.

When the display panel is used for information display apparatus such as a cell phone, it is preferable to mount (form) the source driver IC (circuit) 14 and gate driver IC (circuit) 12 on one side of the display panel as shown in Figure 9 (incidentally, a configuration in which driver ICs (circuits) are mounted (formed) on one side of a display panel is referred to as a three-side free configuration (structure). Conventionally, the gate driver IC 12 is mounted on an X side of a display area and a source driver IC 14 is mounted on a Y side). This makes it easy in the design to center the center line of a display screen 50 on the display apparatus and mount the driver ICs. Using the three-side free configuration, the gate driver circuit may be produced by high-temperature polysilicon technology, low-temperature polysilicon technology or the like (i.e., at least one of the source driver

circuit 14 and gate driver circuit 12 may be formed directly on the board 71 by polysilicon technology).

Incidentally, the three-side free configuration includes not only a configuration in which ICs are placed or formed directly on the board 71, but also a configuration in which a film (TCP, TAB, or other technology) with a source driver IC (circuit) 14 and gate driver IC (circuit) 12 mounted are pasted on one side (or almost one side) of the board 71. That is, the three-side free configuration includes configurations and arrangements in which two sides are left free of ICs and all similar configurations.

If the gate driver circuit 12 is placed beside the source driver circuit 14 as shown in Figure 9, the gate signal line 17 must be formed along the side C.

Incidentally, the thick solid line in Figure 9, etc. indicates gate signal lines 17 formed in parallel. Thus, as many gate signal lines 17 as there are scanning signal lines are formed in parallel in part b (bottom of the screen) while a single gate signal line 17 is formed in part a (top of the screen).

Spacing between the gate signal lines 17 formed on the side C is from 5 μm to 12 μm (both inclusive). If it is less than 5 μm, parasitic capacitance will cause noise on adjacent gate signal lines. It has been shown experimentally that parasitic capacitance has significant effects when the spacing

is 7 μm or less. Furthermore, when the spacing is less than

5 μm, beating noise and other image noise appear intensely

on the display screen. In particular, noise generation

differs between the right and left sides of the screen and

it is difficult to reduce the beating noise and other image

noise. When the spacing exceeds 12 μm, bezel width D of the

display panel becomes too large to be practical.

To reduce the image noise, a ground pattern (conductive

pattern which has been fixed at a constant voltage or set

generally at a stable potential) can be placed under or above

the gate signal lines 17. Alternatively, a separate shield

plate (shield foil: a conductive pattern which has been fixed

at a constant voltage or set generally at a stable potential)

may be placed on the gate signal lines 17.

The gate signal lines 17 on the side C in Figure 9 may

be formed of ITO electrodes. However, to reduce resistance,

preferably they are formed by laminating ITO and thin metal

films. Also preferably they are formed of metal films. When

using an ITO laminate, a titanium film is formed on the ITO,

and a thin aluminum film or aluminum-molybdenum alloy film

is formed on it. Alternatively, a chromium is formed on the

ITO. For metal films, thin aluminum films or chromium films

are used. This also applies to other examples of the present

invention.

Incidentally, although it has been stated with reference to Figure 9 and the like that the gate signal lines 17 are placed on one side of the display area, this is not restrictive and they may be placed on both sides. For example, the gate signal line 17a may be placed (formed) on the right side of the display screen 50 while the gate signal line 17b may be placed (formed) on the left side of the display screen 50. This also applies to other examples.

Also, the source driver IC 14 and gate driver IC 12 may be integrated into a single chip. Then, it suffices to mount only one IC chip on the display panel. This also reduces implementation costs. Furthermore, this makes it possible to simultaneously generate various voltages for use in the single-chip driver IC.

Incidentally, although it has been stated that the source driver IC 14 and gate driver IC 12 are made of silicon or other semiconductor wafers and mounted on the display panel, this is not restrictive. Needless to say, they may be formed directly on the display panel 82 using low-temperature polysilicon technology or high-temperature polysilicon technology.

Although it has been stated that pixels are of the three primary colors of R, G, and B, this is not restrictive. They may be of three colors of cyan, yellow, and magenta. They may be of two colors of B and yellow. Of course, they may

be monochromatic. Alternatively, they may be of six colors of R, G, B, cyan, yellow, and magenta or of five colors of R, G, B, cyan, and magenta. These are natural colors which provide an expanded color reproduction range, enabling good display. Thus, the EL display apparatus according to the present invention is not limited to those which provide color display using the three primary colors of R, G, and B.

Mainly three methods are available to colorize an organic EL display panel. One of them is a color conversion method. It suffices to form a single layer of blue as a light-emitting layer. The remaining green and red colors needed for full color display can be produced from the blue color through color conversion. Thus, this method has the advantage of eliminating the need to paint the R, G, and B colors separately and prepare organic EL materials for the R, G, and B colors. The color conversion method does not lower yields unlike the multi-color painting method. Any of the three methods can be applied to the EL display panel of the present invention.

Also, in addition to the three primary colors, white light-emitting pixels may be formed. The white light-emitting pixels can be created (formed or constructed) by laminating R, G, and B light-emitting structures. A set of pixels consists of pixels for the three primary colors RGB and a white light-emitting pixel 16W. Forming the white light-emitting pixels makes it easier to express peak

brightness of white, and thus possible to implement bright image display.

Even when using a set of pixels for the three primary colors RGB, it is preferable to vary pixel electrode areas for the different colors. Of course, an equal area may be used if luminous efficiencies of the different colors as well as color purity are well balanced. However, if one or more colors are poorly balanced, preferably the pixel electrodes (light-emitting areas) are adjusted. The electrode area for each color can be determined based on current density. That is, when white balance is adjusted in a color temperature range of 7000 K (Kelvin) to 12000 K (both inclusive), difference between current densities of different colors should be within ±30%. More preferably, the difference should be within ±15%. For example, if current densities are around 100 A/square meter, all the three primary colors should have a current density of 70 A/square meter to 130 A/square meter (both inclusive). More preferably, all the three primary colors should have a current density of 85 A/square meter to 115 A/square meter (both inclusive).

The EL element 15 is a self-luminous element. When light from this self-luminous element enters a transistor serving as a switching element, a photoconductive phenomenon occurs. The photoconductive phenomenon is a phenomenon in which leakage

(off-leakage) increases due to photoexcitation when a switching element such as a transistor is off.

To deal with this problem, the present invention forms a shading film under the gate driver 12 (source driver 14 in some cases) and under the pixel transistor 11. The shading film is formed of thin film of metal such as chromium and is from 50 nm to 150 nm thick (both inclusive). A thin film will provide a poor shading effect while a thick film will cause irregularities, making it difficult to pattern the transistor 11A1 in an upper layer.

In the case of the driver circuit 12 and the like, it is necessary to reduce penetration of light not only from the topside, but also from the underside. This is because the photoconductive phenomenon will cause malfunctions. If cathode electrodes are made of metal films, the present invention also forms a cathode electrode on the surface of the driver 12 and the like and uses it as a shading film.

However, if a cathode electrode is formed on the driver 12, electric fields from the cathode electrode may cause driver malfunctions or place the cathode electrode and driver circuit in electrical contact. To deal with this problem, the present invention forms at least one layer of organic EL film, and preferably two or more layers, on the driver circuit 12 simultaneously with the formation of organic EL film on the pixel electrode.

If a short circuit occurs between terminals of one or more transistors 11 or between a transistor 11 and signal line in the pixel, the EL element 15 may become a bright spot which remains illuminated constantly. The bright spot is visually conspicuous and must be turned into a black spot (turned off). The pixel 16 which corresponds to the bright spot is detected and the capacitor 19 is irradiated with laser light to cause a short circuit across the capacitor. As a result, the capacitor 19 can no longer hold electric charges, and thus the transistor 11a can be stopped from passing current. It is desirable to remove that part of a cathode film which will be irradiated with laser light to prevent the laser irradiation from causing a short circuit between a terminal electrode of the capacitor 19 and the cathode film.

Flaws in a transistor 11 in the pixel 16 will affect the source driver IC 14 and the like. For example, if a source-drain (SD) short circuit 562 occurs in the driver transistor 11a in Figure 56, a Vdd voltage of the panel is applied to the source driver IC 14. Thus, preferably the power supply voltage of the source driver IC 14 is kept equal to or higher than the power supply voltage Vdd of the panel. Preferably, the reference voltage used by the source driver IC 14 can be adjusted with an electronic regulator 561 (See Figure 148).

If an SD short circuit 562 occurs in the transistor 11a, an excessive current flows through the EL element 15. In other words, the EL element 15 remains illuminated constantly (becomes a bright spot). The bright spot is conspicuous as a defect. For example, if a source-drain (SD) short circuit occurs in the transistor 11a in Figure 56, current flows constantly from the Vdd voltage to the EL element 15 (when the transistor 11d is on) regardless of the magnitude of gate (G) terminal voltage of the transistor 11a. Thus, a bright spot results.

On the other hand, if an SD short circuit occurs in the transistor 11a and if the transistor 11c is on, the Vdd voltage is applied to the source signal line 18 and to the source driver 14. If the power supply voltage of the source driver 14 is not higher than Vdd, voltage resistance may be exceeded, causing the source driver 14 to rupture. Thus, it is preferable that the power supply voltage of the source driver 14 is equal to or higher than the Vdd voltage (the higher voltage of the panel).

An SD short circuit of the transistor 11a may go beyond a point defect and lead to rupture of the source driver circuit of the panel. Also, the bright spot is conspicuous, which makes the panel defective. Thus, it is necessary to turn the bright spot into a black spot by cutting the wiring which connects between the transistor 11 and EL element 15.

Preferably an optical means such as laser light is used to cut the wiring.

A drive method according to the present invention will be described below. As shown in Figure 1, the gate signal line 17a conducts when the row remains selected (since the transistor 11 in Figure 1 is a P-channel transistor, the gate signal line 17a conducts when it is in low state) and the gate signal line 17b conducts when the row remains non-selected.

Parasitic capacitance (not shown) is present in the source signal line 18. The parasitic capacitance is caused by the capacitance at the junction of the source signal line 18 and gate signal line 17, channel capacitance of the transistors 11b and 11c, etc.

The time t required to change the current value of the source signal line 18 is given by $t = C \cdot V/I$, where C is stray capacitance, V is a voltage of the source signal line, and I is a current flowing through the source signal line. Thus, if the current value can be increased tenfold, the time required to change the current value can be reduced nearly tenfold. This also means that the current value can be changed to a predetermined value even if the parasitic capacitance of the source signal line 18 is increased tenfold. Thus, to apply a predetermined current value during a short horizontal scanning period, it is useful to increase the current value.

When input current is increased tenfold, output current is also increased tenfold, resulting in a tenfold increase in the EL brightness. Thus, to obtain predetermined brightness, a light emission period is reduced tenfold by reducing the conduction period of the transistor 17d in Figure 1 tenfold compared to a conventional conduction period. Incidentally, the tenfold increases/decreases are cited as an example to facilitate understanding and are not meant to be restrictive.

Thus, in order to charge and discharge the parasitic capacitance of the source signal line 18 sufficiently and program a predetermined current value into the transistor 11a of the pixel 16, it is necessary to output a relatively large current from the source driver 14. However, when such a large current is passed through the source signal line 18, its current value is programmed into the pixel and a current larger than the predetermined current flows through the EL element 15. For example, if a 10 times larger current is programmed, naturally a 10 times larger current flows through the EL element 15 and the EL element 15 emits 10 times brighter light. To obtain predetermined emission brightness, the time during which the current flows through the EL element 15 can be reduced tenfold. This way, the parasitic capacitance can be charged/discharged sufficiently from the source signal line 18 and the predetermined emission brightness can be obtained.

Incidentally, although it has been stated that a 10 times larger current value is written into the pixel transistor 11a (more precisely, the terminal voltage of the capacitor 19 is set) and that the conduction period of the EL element 15 is reduced to 1/10, this is only exemplary. In some cases, a 10 times larger current value may be written into the pixel transistor 11a and the conduction period of the EL element 15 may be reduced to 1/5. On the other hand, a 10 times larger current value may be written into the pixel transistor 11a and the conduction period of the EL element 15 may be halved.

The present invention is characterized in that the write current into a pixel is set at a value other than a predetermined value and that a current is passed through the EL element 15 intermittently. For ease of explanation, it has been stated herein that an N times larger current is written into the pixel transistor 11 and the conduction period of the EL element 15 is reduced to 1/N. However, this is not restrictive. Needless to say, N1 times larger current may be written into the pixel transistor 11 and the conduction period of the EL element 15 may be reduced to 1/N2 (N1 and N2 are different from each other).

In white raster display, it is assumed that average brightness over one field (frame) period of the display screen 50 is B0. This drive method performs current (voltage) programming in such a way that the brightness B1 of each pixel 16 is higher than the average brightness B0. Also, a

non-display area 53 appears during at least one field (frame) period. Thus, in the drive method according to the present invention, the average brightness over one field (frame) period is lower than B1.

Incidentally, the non-display area 52 and display area 53 are not necessarily spaced equally. For example, they may appear at random (provided that the display period or non-display period makes up a predetermined value (constant ratio) as a whole). Also, display periods may vary among R, G, and B.

That is, display periods of R, G, and B or non-display periods can be adjusted (set) to predetermined values (proportions) in such a way as to obtain an optimum white balance.

To facilitate explanation of the drive method according to the present invention, it is assumed that "1/N" means reducing 1F (one field or one frame) to 1/N. Needless to say, however, it takes time to select one pixel row and to program current values (normally, one horizontal scanning period (1 H)) and error may result depending on scanning conditions.

For example, the EL element 15 may be illuminated for 1/5 of a period by programming the pixel 16 with an N = 10 times larger current. The EL element 15 illuminates 10/5 = 2 times more brightly. It is also possible to program an N = 2 times larger current into the pixel 16 and illuminate the

EL element 15 for 1/4 of the period. The EL element 15 illuminates 2/4 = 0.5 time more brightly. In short, the present invention achieves display other than constant display (1/1, i.e., non-intermittent display) by using a current other than an N = 1 time current for current programming. Also, the drive system turns off the current supplied to the EL element 15, at least once during one frame (or one field) period. Also, the drive system at least achieves intermittent display by programming the pixel 16 with a current larger than a predetermined value.

A problem with an organic (inorganic) EL display is that it uses a display method basically different from that of an CRT or other display which presents an image as a set of displayed lines using an electron gun. That is, the EL display holds the current (voltage) written into a pixel for 1F (one field or one frame) period. Thus, a problem is that displaying moving pictures will result in blurred edges.

According to the present invention, current is passed through the EL element 15 only for a period of 1F/N, but current is not passed during the remaining period (1F (N − 1) /N). Let us consider a situation in which the drive system is implemented and one point on the screen is observed. In this display condition, image data display and black display (non-illumination) are repeated every 1F. That is, image data is displayed intermittently in the temporal sense. When

moving picture data are displayed intermittently, a good display condition is achieved without edge blur. In short, movie display close to that of a CRT can be achieved.

The drive method according to the present invention implements intermittent display. However, the intermittent display can be achieved by simply turning on and off the transistor 11d on a 1-H cycle. Consequently, a main clock of the circuit does not differ from conventional ones, and thus there is no increase in the power consumption of the circuit. Liquid crystal display panels need an image memory in order to achieve intermittent display. According to the present invention, image data is held in each pixel 16. Thus, the present invention requires no image memory for intermittent display.

The present invention controls the current passed through the EL element 15 by simply turning on and off the switching transistor 11d, the transistor 11e, and the like. That is, even if the current Iw flowing through the EL element 15 is turned off, the image data is held as it is in the capacitor 19. Thus, when the transistor 11d is turned on the next time, the current passed through the EL element 15 has the same value as the current flowing through the EL element 15 the previous time. Even to achieve black insertion (intermittent display such as black display), the present invention does not need to speed up the main clock of the circuit. Also, it does not

need to elongate a time axis, and thus requires no image memory.
Besides, the EL element 15 responds quickly, requiring a short
time from application of current to light emission. Thus,
the present invention is suitable for movie display, and by
using intermittent display, it can solve a problem with
conventional data-holding display panels (liquid crystal
display panels, EL display panels, etc.) in displaying moving
pictures.

Furthermore, in a large display apparatus, if increased
wiring length of the source signal line 18 results in increased
parasitic capacitance in the source signal line 18, this can
be dealt with by increasing the value of N. When the value
of programming current applied to the source signal line 18
is increased N times, the conduction period of the gate signal
line 17b (the transistor 11d) can be set to 1F/N. This makes
it possible to apply the present invention to television sets,
monitors, and other large display apparatus.

The output stage of the source driver circuit 14 is
constituted of a constant-current circuit 704 (see Figure 70).
The constant-current circuit eliminates the need to vary buffer
size of the output stage according to the size of the display
panel unlike the source driver circuits of liquid crystal
display panels.

The drive method according to the present invention will
be described with reference to drawings in more detail below.

The parasitic capacitance of the source signal line 18 is generated by the coupling capacitance with adjacent source signal lines 18, buffer output capacitance of the source driver IC (circuit) 14, cross capacitance between the source signal line 18 and gate signal line 17, etc. This parasitic capacitance is normally 10 pF or larger. In the case of voltage driving, since voltage is applied to the source signal line 18 from the source driver IC 14 at low impedance, more or less large parasitic capacitance does not disturb driving.

However, in the case of current driving, especially image display at the black level, the pixel capacitor 19 needs to be programmed with a minute current of 20 nA or less. Thus, if parasitic capacitance larger than a predetermined value is generated, the parasitic capacitance cannot be charged and discharged during the time when one pixel row is programmed (normally within 1 H, but not limited to 1 H because two pixel rows may be programmed simultaneously). If the parasitic capacitance cannot be charged and discharged within a period of 1 H, sufficient current cannot be written into the pixel, resulting in inadequate resolution.

In the pixel configuration in Figure 1, the programming current Iw flows through the source signal line 18 during current programming as shown in figure 3(a). The current Iw flows through the transistor 11a and voltage is set

(programmed) in the capacitor 19 in such a way as to maintain the current Iw. At this time, the transistor 11d is open (off).

During a period when the current flows through the EL element 15, the transistors 11c and 11b turn off and the transistor 11d turns on as shown in Figure 3(b). Specifically, a turn-off voltage (Vgh) is applied to the gate signal line 17a, turning off the transistors 11b and 11c. On the other hand, a turn-on voltage (Vgl) is applied to the gate signal line 17b, turning on the transistor 11d.

Suppose a current I1 is N times the current which should normally flow (a predetermined value), the current flowing through the EL element 15 in Figure 3(b) is also Iw. Thus, the EL element 15 emits light 10 times more brightly that a predetermined value. In other words, as shown in Figure 12, the larger the magnification N, the higher the display brightness B of the pixel 16. Thus, the magnification N and the brightness of the pixel 16 are proportional to each other.

If the transistor 11d is kept on for a period 1/N the period during which it is normally kept on (approximately 1F) and is kept off during the remaining period (N - 1)/N, the average brightness over the 1F equals predetermined brightness. This display condition closely resembles the display condition under which a CRT is scanning a screen with an electronic gun. The difference is that 1/N of the entire screen illuminates

(where the entire screen is taken as 1) (in a CRT, what illuminates is one pixel row--more precisely, one pixel).

According to the present invention, 1F/N of the image display area 53 moves from top to bottom of the screen 50 as shown in Figure 13(b). According to the present invention, current flows through the EL element 15 only for the period of 1F/N, but current does not flow during the remaining period $(1F \cdot (N - 1)/N)$. Thus, the pixel is displayed intermittently. However, due to an afterimage, the entire screen appears to be displayed uniformly to the human eye.

Incidentally, as shown in Figure 13, the write pixel row 51a is non-illuminated 52a. However, this is true only to the pixel configurations in Figures 1, 2, etc. In the pixel configuration of a current mirror shown in Figure 38, etc., the write pixel row 51a may be illuminated. However, description will be given herein citing mainly the pixel configuration in Figure 1 for ease of explanation. A drive method which involves driving a pixel intermittently by programming it with a current larger than the predetermined drive current Iw shown in Figures 13, 16, etc. is referred to as N-fold pulse driving.

In this display condition, image data display and black display (non-illumination) are repeated every 1F. That is, image data is displayed at intervals (intermittently) in the temporal sense. Liquid crystal display panels (EL display

panels other than that of the present invention), which hold data in pixels for a period of 1F, cannot keep up with changes in image data during movie display, resulting is blurred moving pictures (edge blur of images). Since the present invention displays images intermittently, it can achieve a good display condition without edge blur of images. In short, movie display close to that of a CRT can be achieved.

Incidentally, to drive the pixel 16 as shown in Figure 13, it is necessary to be able to separately control the current programming period of the pixel 16 (in the configuration shown in Figure 1, the period during which the turn-on voltage Vgl is applied to the gate signal line 17a) and the period when the EL element 15 is under on/off control (in the pixel configuration shown in Figure 1, the period during which the turn-on voltage Vgl or turn-off voltage Vgh is applied to the gate signal line 17b). Thus, the gate signal line 17a and gate signal line 17b must be separated.

For example, when only a single gate signal line 17 is laid from the gate driver circuit 12 to the pixel 16, the drive method according to the present invention cannot be implemented using a configuration in which logic (Vgh or Vgl) applied to the gate signal line 17 is applied to the transistor 11b and the logic applied to the gate signal line 17 is converted (Vgh or Vgl) by an inverter and applied to the transistor 11d. Thus, the present invention requires a gate driver circuit 12a which

operates the gate signal line 17a and gate driver circuit 12b which operates the gate signal line 17b.

Besides, the drive method according to the present invention provides a non-illuminated display even with the pixel configuration shown in Figure 1 during periods other than the current programming period (1 H).

A timing chart of the drive method shown in Figure 13 is illustrated in Figure 14. The pixel configuration referred to in the present invention and the like is the one shown in Figure 1 unless otherwise stated. As can be seen from Figure 14, in each selected pixel row (the selection period is designated as 1 H), when a turn-on voltage (Vgl) is applied to the gate signal line 17a (see Figure 14(a)), a turn-off voltage (Vgh) is applied to the gate signal line 17b (see Figure 14(b)). During this period, current does not flow through the EL element 15 (non-illumination mode). In a non-selected pixel row, a turn-on voltage (Vgl) is applied to the gate signal line 17b and a turn-off voltage (Vgh) is applied to the gate signal line 17a. During this period, current flows through the EL element 15 (illumination mode). In the illumination mode, the EL element 15 illuminates at a brightness (N·B) N times the predetermined brightness and the illumination period is 1F/N. Thus, the average display brightness of the display panel over 1F is given by (N·B) × (1/N) = B (the predetermined brightness).

Figure 15 shows an example in which operations shown in Figure 14 are applied to each pixel row. The figure shows voltage waveforms applied to the gate signal lines 17. Waveforms of the turn-off voltage are denoted by Vgh (high level) while waveforms of the turn-on voltage are denoted by Vgl (low level). The subscripts such as (1) and (2) indicate selected pixel row numbers.

In Figure 15, a gate signal line 17a(1) is selected (Vgl voltage) and a programming current flows through the source signal line 18 in the direction from the transistor 11a in the selected pixel row to the source driver circuit 14. The programming current is N times larger than a predetermined value (for ease of explanation, it is assumed that N = 10. Of course, since the predetermined value is a data current for use to display images, it is not a fixed value unless in the case of white raster display). Therefore, the capacitor 19 is programmed so that a 10 times larger current will flow through the transistor 11a. When the pixel row (1) is selected, in the pixel configuration shown in Figure 1, a turn-off voltage (Vgh) is applied to the gate signal line 17b(1) and current does not flow through the EL element 15.

After 1 H, a gate signal line 17a(2) is selected (Vgl voltage) and a programming current flows through the source signal line 18 in the direction from the transistor 11a in the selected pixel row to the source driver circuit 14. The

programming current is N times larger than a predetermined

value (for ease of explanation, it is assumed that N = 10).

Therefore, the capacitor 19 is programmed so that 10 times

larger current will flow through the transistor 11a. When

the pixel row (2) is selected, in the pixel configuration shown

in Figure 1, a turn-off voltage (Vgh) is applied to the gate

signal line 17b(2) and current does not flow through the EL

element 15. However, since a turn-off voltage (Vgh) is applied

to the gate signal line 17a(1) and a turn-on voltage (Vgl)

is applied to the gate signal line 17b(1) of the pixel row

(1), the EL element 15 illuminates.

After the next 1 H, a gate signal line 17a(3) is selected,

a turn-off voltage (Vgh) is applied to the gate signal line

17b(3), and current does not flow through the EL element 15

in the pixel row (3). However, since a turn-off voltage (Vgh)

is applied to the gate signal lines 17a(1) and (2) and a turn-on

voltage (Vgl) is applied to the gate signal lines 17b(1) and

(2) in the pixel rows (1) and (2), the EL element 15 illuminates.

Through the above operation, images are displayed in sync

with a synchronization signal of 1 H. However, with the drive

method in Figure 15, a 10 times larger current flows through

the EL element 15. Thus, the display screen 50 is 10 times

brighter. Of course, it goes without saying that for display

at a predetermined brightness in this state, the programming

current can be reduced to 1/10. However, a 10 times smaller

current will cause a shortage of write current due to parasitic capacitance. Thus, the basic idea of the present invention is to use a large current for programming, insert a non-display area 52, and thereby obtain a predetermined brightness.

Incidentally, the drive method according to the present invention causes a current larger than a predetermined current to flow through the EL element 15, and thereby charges and discharges the parasitic capacitance of the source signal line 18 sufficiently. That is, there is no need to pass an N times larger current through the EL element 15. For example, it is conceivable to form a current path in parallel with the EL element 15 (form a dummy EL element and use a shield film to prevent the dummy EL element from emitting light) and divide the flow of current between the EL element 15 and the dummy EL element. For example, when a signal current is 0.2 µA, a programming current is set to 2.2 µA and the current of 2.2 µA is passed through the transistor 11a. Then, the signal current of 0.2 µA may be passed through the EL element 15 and 2 µA may be passed through the dummy EL element, for example. That is, the dummy pixel row 281 in Figure 27 remains selected constantly. Incidentally, the dummy pixel row is either kept from emitting light or hidden from view by a shield film or the like even if it emits light.

With the above configuration, by increasing the current passed through the source signal line 18 N times, it is possible

to pass an N times larger current through the driver transistor 11a and pass a current sufficiently smaller than the N times larger current through the EL element 15. As shown in Figure 5, this method allows the entire display screen 50 to be used as the image display area 53 without a non-display area 52.

Figure 13(a) shows writing into the display screen 50. In Figure 13(a), reference numeral 51a denotes a write pixel row. A programming current is supplied to the source signal line 18 from the source driver IC 14. In Figure 13 and the like, there is one pixel row into which current is written during a period of 1 H, but this is not restrictive. The period may be 0.5 H or 2 Hs. Also, although it has been stated that a programming current is written into the source signal line 18, the present invention is not limited to current programming. The present invention may also use voltage programming (Figure 62, etc.) which writes voltage into the source signal line 18.

In Figure 13(a), when the gate signal line 17a is selected, the current to be passed through the source signal line 18 is programmed into the transistor 11a. At this time, a turn-off voltage is applied to the gate signal line 17b, and current does not flow through the EL element 15. This is because when the transistor 11d is on on the EL element 15, a capacitance component of the EL element 15 is visible from the source signal line 18 and the capacitance prevents sufficient current from

being programmed into the capacitor 19. Thus, to take the configuration shown in Figure 1 as an example, the pixel row into which current is written is a non-illuminated area 52 as shown in Figure 13(b).

Suppose an N times larger current is used for programming (it is assumed that N = 10 as described above), the screen becomes 10 times brighter. Thus, 90% of the display screen 50 can be constituted of the non-illuminated area 52. Thus, for example, if the number of horizontal scanning lines in the screen display area is 220 (S = 220) in compliance with QCIF, 22 horizontal scanning lines can compose a display area 53 while 220 - 22 = 198 horizontal scanning lines can compose a non-display area 52. Generally speaking, if the number of horizontal scanning lines (number of pixel rows) is denoted by S, S/N of the entire area constitutes a display area 53, which is illuminated N times more brightly. Then, the display area 53 is scanned in the vertical direction of the screen. Thus, S (N - 1)/N of the entire area is a non-illuminated area 52. The non-illuminated area presents a black display (is non-luminous). Also, the non-luminous area 52 is produced by turning off the transistor 11d. Incidentally, although it has been stated that the display area 53 is illuminated N times more brightly, naturally the value of N is adjusted by brightness adjustment and gamma adjustment.

In the above example, if a 10 times larger current is used for programming, the screen becomes 10 times brighter and 90% of the display screen 50 can be constituted of the non-illuminated area 52. However, this does not necessarily mean that R, G, and B pixels constitute the non-illuminated area 52 in the same proportion. For example, 1/8 of the R pixels, 1/6 of the G pixels, and 1/10 of the B pixels may constitute the non-illuminated area 52 with different colors making up different proportions. It is also possible to allow the non-illuminated area 52 (or illuminated area 53) to be adjusted separately among R, G, and B. For that, it is necessary to provide separate gate signal lines 17b for R, G, and B. However, allowing R, G, and B to be adjusted separately makes it possible to adjust white balance, making it easy to adjust color balance for each gradation (see Figure 41).

As shown in Figure 13(b), pixel rows including the write pixel row 51a compose a non-illuminated area 52 while an area of S/N (1F/N in the temporal sense) above the write pixel row 51a compose a display area 53 (when write scans are performed from top to bottom of the screen. When the screen is scanned from bottom to top, the areas change places). Regarding the display condition of the screen, a strip of the display area 53 moves from top to bottom of the screen.

In Figure 13, one display area 53 moves from top to bottom of the screen. At a low frame rate, the movement of the display area 53 is recognized visually. It tends to be recognized easily especially when a user closes his/her eyes or moves his/her head up and down.

To deal with this problem, the display area 53 can be divided into a plurality of parts as shown in Figure 16. If the total area of the divided display area is S (N - 1)/N, the brightness is equal to the brightness in Figure 13. Incidentally, there is no need to divide the display area 53 equally. Also, there is no need to divide the non-display area 52 equally.

Dividing the display area 53 reduces flickering of the screen. Thus, a flicker-free good image display can be achieved. Incidentally, the display area 53 may be divided more finely. However, the more finely the display area 53 is divided, the poorer the movie display performance becomes.

Figure 17 shows voltage waveforms of gate signal lines 17 and emission brightness of the EL element. As can be seen from Figure 17, a period (1F/N) during which the gate signal line 17b is set to Vg1 is divided into a plurality of parts (K parts). That is, a period of 1F/(K·N) during which the gate signal line 17b is set to Vg1 repeats K times. This reduces flickering and implements image display at a low frame rate. Preferably, the number of divisions is variable. For example,

when the user presses a brightness adjustment switch or turns a brightness adjustment knob, the value of K may be changed in response. Also, the user may be allowed to adjust brightness. Alternatively, the value of K may be changed manually or automatically depending on images or data to be displayed.

Incidentally, although it has been stated with reference to Figure 17 and the like that a period (1F/N) during which the gate signal line 17b is set to Vg1 is divided into a plurality of parts (K parts) and that a period of 1F/(K·N) during which the gate signal line 17b is set to Vg1 repeats K times, this is not restrictive. A period of 1F/(K·N) may be repeated L (L ≠ K) times. In other words, the present invention displays the display screen 50 by controlling the period (time) during which current is passed through the EL element 15. Thus, the idea of repeating the 1F/(K·N) period L (L ≠ K) times is included in the technical idea of the present invention. Also, by varying the value of L, the brightness of the display screen 50 can be changed digitally. For example, there is a 50% change of brightness (contrast) between L = 2 and L = 3. Also, when dividing the image display area 53, the period when the gate signal line 17b is set to Vg1 does not necessarily need to be divided equally.

In the example described above, the display screen 50 is turned on and off (illuminated and non-illuminated) as the current delivered to the EL element 15 is switched on and off.

That is, approximately equal current is passed through the transistor 11a multiple times using electric charges held in the capacitor 19. The present invention is not limited to this. For example, the display screen 50 may be turned on and off (illuminated and non-illuminated) by charging and discharging the capacitor 19.

Figure 18 shows voltage waveforms applied to gate signal lines 17 to achieve the image display condition shown in Figure 16. Figure 18 differs from Figure 15 in the operation of the gate signal line 17b. The gate signal line 17b is turned on and off (Vgl and Vgh) as many times as there are screen divisions. Figure 18 is the same as Figure 15 in other respects, and thus description thereof will be omitted.

Since black display on EL display apparatus corresponds to complete non-illumination, contrast does not lower unlike in the case of intermittent display on liquid crystal display panels. Also, with the configurations in Figure 1, intermittent display can be achieved by simply turning on and off the transistor 11d. With the configurations in Figures 38, and 51, intermittent display can be achieved by simply turning on and off the transistor element 11e. This is because image data is stored in the capacitor 19 (the number of gradations is infinite because analog values are used). That is, the image data is held in each pixel 16 for a period of 1F. Whether to deliver a current which corresponds to the

stored image data to the EL element 15 is controlled by controlling the transistors 11d and 11e.

Thus, the drive method described above is not limited to a current-driven type and can be applied to a voltage-driven type as well. That is, in a configuration in which the current passed through the EL element 15 is stored in each pixel, intermittent driving is implemented by switching on and off the current path between the driver transistor 11 and EL element 15.

It is important to maintain terminal voltage of the capacitor 19. This is because if the terminal voltage of the capacitor 19 changes (charge/discharge) during one field (frame) period, flickering occurs when the screen brightness changes and the frame rate lowers. The current passed through the EL element 15 by the transistor 11a must be higher than 65%. More specifically, if the initial current written into the pixel 16 and passed through the EL element 15 is taken as 100%, the current passed through the EL element 15 just before it is written into the pixel 16 in the next frame (field) must not fall below 65%.

With the pixel configuration shown in Figure 1, there is no difference in the number of transistors 11 in a single pixel between when an intermittent display is created and when an intermittent display is not created. That is, leaving the pixel configuration as it is, proper current programming is

achieved by removing the effect of parasitic capacitance of the source signal line 18. Besides, movie display close to that of a CRT is achieved.

Also, since the operation clock of the gate driver circuit 12 is significantly slower than the operation clock of the source driver circuit 14, there is no need to upgrade the main clock of the circuit. Besides, the value of N can be changed easily.

Incidentally, the image display direction (image writing direction) may be from top to bottom of the screen in the first field (frame), and from bottom to top of the screen in the second field (frame). That is, an upward direction and downward direction may be repeated alternately.

Alternatively, it is possible to use a downward direction in the first field (frame), turn the entire screen into black display (non-display) once, and use an upward direction in the second field (frame). It is also possible to turn the entire screen into black display (non-display) once.

Incidentally, although top-to-bottom and bottom-to-top writing directions on the screen are used in the drive method described above, this is not restrictive. It is also possible to fix the writing direction on the screen to a top-to-bottom direction or bottom-to-top direction and move the non-display area 52 from top to bottom in the first field, and from bottom to top in the second field. Alternatively, it is possible

to divide a frame into three fields and assign the first field
to R, the second field to G, and the third field to B so that
three fields compose a single frame. It is also possible to
display R, G, and B in turns by switching among them every
horizontal scanning period (1 H) (see Figures 175 to 180 and
their description). The items mentioned above also apply to
other examples of the present invention.

The non-display area 52 need not be totally
non-illuminated. Weak light emission or dim image display
will not be a problem in practical use. It should be regarded
to be an area which has a lower display brightness than the
image display area 53. Also, the non-display area 52 may be
an area which does not display one or two colors out of R,
G, and B. Also, it may be an area which displays one or two
colors among R, G, and B at low brightness.

Basically, if the brightness of the display area 53 is
kept at a predetermined value, the larger the display area
53, the brighter the display screen 50. For example, when
the brightness of the image display area 53 is 100 (nt), if
the percentage of the display screen 50 accounted for by the
display area 53 changes from 10% to 20%, the brightness of
the screen is doubled. Thus, by varying the proportion of
the display area 53 in the entire screen 50, it is possible
to vary the display brightness of the screen. The display

brightness of the screen 50 is proportional to the ratio of the display area 53 to the screen 50.

The size of the display area 53 can be specified freely by controlling data pulses (ST2) sent to the shift register circuit 61. Also, by varying the input timing and period of the data pulses, it is possible to switch between the display condition shown in Figure 16 and display condition shown in Figure 13. Increasing the number of data pulses in one IF period makes the screen 50 brighter and decreasing it makes the screen 50 dimmer. Also, continuous application of the data pulses brings on the display condition shown in Figure 13 while intermittent application of the data pulses brings on the display condition shown in Figure 16.

Figure 19(a) shows a brightness adjustment scheme used when the display area 53 is continuous as in Figure 13. The display brightness of the screen 50 in Figure 19(a1) is the brightest, the display brightness of the screen 50 in Figure 19(a2) is the second brightest, and display brightness of the screen 50 in Figure 19(a3) is the dimmest. Figure 19(a) is most suitable for movie display.

Changes from Figure 19(a1) to Figure 19(a3) (or vice versa) can be achieved easily by controlling the shift register circuit 61 and the like of the gate driver circuit 12 as described above. In this case, there is no need to vary the Vdd voltage in Figure 1. That is, the brightness of the screen 50 can

be varied without changing the power supply voltage. Also, in the process of change from Figure 19(a1) to Figure 19(a3), the gamma characteristics of the screen do not change at all. Thus, the contrast and gradation characteristics of the display screen are maintained regardless of the brightness of the screen 50. This is an effective feature of the present invention.

In brightness adjustment of a conventional screen, low brightness of the screen 50 results in poor gradation performance. That is, even if 64 gradations can be displayed in a high-brightness display, in most cases, less than half the gradations can be displayed in a low-brightness display. In contrast, the drive method according to the present invention does not depend on the display brightness of the screen and can display up to 64 gradations, which is the highest.

Figure 19(b) shows a brightness adjustment scheme used when the display areas 53 are scattered as in Figure 16. The display brightness of the screen 50 in Figure 19(b1) is the brightest, the display brightness of the screen 50 in Figure 19(b2) is the second brightest, and display brightness of the screen 50 in Figure 19(b3) is the dimmest. Changes from Figure 19(b1) to Figure 19(b3) (or vice versa) can be achieved easily by controlling the shift register circuit 61 of the gate driver circuit 12 and the like as described above. By scattering

the display areas 53 as shown in Figure 19(b), it is possible to eliminate flickering even at a low frame rate.

To eliminate flickering at an even lower frame rate, the display areas 53 can be scattered more finely as shown in Figure 19(c). However, this lowers movie display performance. Thus, the drive method in Figure 19(a) is suitable for moving pictures. The drive method in Figure 19(c) is suitable when it is desired to reduce power consumption by displaying still pictures. Switching from Figure 19(a) to Figure 19(c) can be done easily by controlling the shift register circuit 61.

Mainly, N = two times, N = 4 times, etc. are used in the above example. Needless to say, however, the present invention is not limited to integral multiples. It is not limited to a value equal to or larger than N = two, either. For example, less than half the screen 50 may be a non-display area 52 at a certain time point. A predetermined brightness can be achieved if a current Iw 5/4 a predetermined value is used for current programming and the EL element is illuminated for 4/5 of 1F.

The present invention is not limited to the above. For example, a current Iw 10/4 a predetermined value may be used for current programming to illuminate the EL element for 4/5 of 1F. In this case, the EL element illuminates at twice a predetermined brightness. Alternatively, a current Iw 5/4 a predetermined value may used for current programming to

illuminate the EL element for 2/5 of 1F. In this case, the EL element illuminates at 1/2 the predetermined brightness. Also, a current Iw 5/4 a predetermined value may be used for current programming to illuminate the EL element for 1/1 of 1F. In this case, the EL element illuminates at 5/4 the predetermined brightness.

Thus, the present invention controls the brightness of the display screen by controlling the magnitude of programming current and illumination period IF. Also, by illuminating the EL element for a period shorter than the period of 1F, the present invention can insert a non-display area 52, and thereby improve movie display performance. By illuminating the EL element constantly for the period of 1F, the present invention can display a bright screen.

If pixel size is A square mm and predetermined brightness of white raster display is B (nt), preferably programming current I (μA) (programming current outputted from the source driver circuit 14) or the current written into the pixel satisfies:

$(A \times B)/20 \leq I \leq (A \times B)$

This provides good light emission efficiency and solves a shortage of write current.

More preferably, the programming current I (μA) falls within the range:

$(A \times B)/10 \leq I \leq (A \times B)$

Figure 20 is an explanatory diagram illustrating another example of increasing the current flowing through a source signal line 18. This method selects a plurality of pixel rows simultaneously, charges and discharges parasitic capacitance and the like of the source signal line 18 using the total current flowing through the plurality of pixel rows, and thereby eases a shortage of write current greatly. Since a plurality of pixel rows are selected simultaneously, drive current per pixel can be reduced. Thus, it is possible to reduce the current flowing through the EL element 15. For ease of explanation, it is assumed that N = 10 (the current passed through the source signal line 18 is increased tenfold).

According to the invention described with reference to Figure 20, M pixel rows are selected simultaneously. A current N times larger than a predetermined current is applied to the source signal line 18 from the source driver IC 14. A current N/M times larger than the current passed through the EL element 15 is programmed into each pixel. As an example, to illuminate the EL element 15 at a predetermined emission brightness, current is passed through the EL element 15 for a duration of M/N the duration of one frame (one field) (M/N is used for ease of explanation and is not meant to be restrictive. As described earlier, it can be specified freely depending on the brightness of the screen 50). This makes it possible to charge and discharge parasitic capacitance of the source signal

line 18 sufficiently, resulting in a sufficient resolution at the predetermined emission brightness.

Current is passed through the EL element 15 only for a period M/N the frame (field) period, but current is not passed during the remaining period (1F (N - 1) M/N). In this display condition, image data display and black display (non-illumination) are repeated every 1F. That is, image data is displayed at intervals (intermittently) in the temporal sense. This achieves a good display condition without edge blur of images. Also, since the source signal line 18 is driven by an N times larger current, it is not affected by parasitic capacitance. Thus, this method can accommodate high-resolution display panels.

Figure 21 is an explanatory diagram illustrating drive waveforms used to implement the drive method shown in Figure 20. Waveforms of the turn-off voltage are denoted by Vgh (H level) while waveforms of the turn-on voltage are denoted by (L level). The subscripts (such as (1), (2), and (3)) indicate pixel row numbers. Incidentally, the number of rows is 220 in the case of a QCIF display panel, and 480 in the case of a VGA display panel.

In Figure 21, a gate signal line 17a(1) is selected (Vgl voltage) and a programming current flows through the source signal line 18 in the direction from the transistor 11a in the selected pixel row to the source driver circuit 14. For

ease of explanation, it is assumed here that the write pixel row 51a is the (1)-th pixel row.

The programming current flowing through the source signal line 18 is N times larger than a predetermined value (for ease of explanation, it is assumed that N = 10. Of course, since the predetermined value is a data current for use to display images, it is not a fixed value unless in the case of white raster display). It is also assumed that five pixel rows are selected simultaneously (M = 5). Therefore, ideally the capacitor 19 of one pixel is programmed so that a twice (N/M = 10/5 = 2) larger current will flow through the transistor 11a.

When the write pixel row is the (1)-th pixel row, the gate signal lines 17a(1), (2), (3), (4), and (5) are selected as shown in Figure 21. That is, the switching transistors 11b and the transistors 11c in the pixel rows (1), (2), (3), (4), and (5) are on. Also, the gate signal lines 17b are 180 degrees out of phase with the gate signal lines 17a. Thus, the switching transistors 11d in the pixel rows (1), (2), (3), (4), and (5) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Ideally, the transistors 11a in the five pixels deliver a current of Iw × 2 each to the source signal line 18 (i.e., a current of Iw × 2 × N = Iw × 2 × 5 = Iw × 10 flows through

the source signal line 18. Thus, if a predetermined voltage Iw flows when the N-fold pulse driving according to the present invention is not used, a current 10 times larger than Iw flows through the source signal line 18).

Through the above operation (drive method), the capacitor 19 of each pixel 16 is programmed with a twice larger current. For ease of understanding, it is assumed here that the transistors 11a have equal characteristics (Vt and S value).

Since five pixel rows are selected simultaneously (M = 5), five driver transistors 11a operate. That is, 10/5 = 2 times larger current flows through the transistor 11a per pixel. The total programming current of the five transistors 11a flows through the source signal line 18. For example, if a current conventionally written into the write pixel row 51a is Iw, a current of Iw × 10 is passed through the source signal line 18. The write pixel rows 51b into which image data is written later than the write pixel row (1) are auxiliary pixel rows used to increase the amount of current delivered to the source signal line 18. However, there is no problem because regular image data is written into the write pixel rows 51b later.

Thus, the four pixel rows 51b provide the same display as the pixel row 51a during a period of 1 H. Consequently, at least the write pixel row 51a and the pixel rows 51b selected to increase current are in non-display mode 52. However, in the pixel configuration of a current mirror, such as shown

in Figure 38, or pixel configuration for voltage programming, the pixel rows may be in display mode.

After 1 H, the gate signal line 17a(1) becomes deselected and a turn-on voltage (Vgl) is applied to the gate signal line 17b. At the same time, the gate signal line 17a(6) is selected (Vgl voltage) and a programming current flows through the source signal line 18 in the direction from the transistor 11a in the selected pixel row (6) to the source driver circuit 14. Through this operation, regular image data is held in the pixel row (1).

After the next 1 H, the gate signal line 17a(2) becomes deselected and a turn-on voltage (Vgl) is applied to the gate signal line 17b. At the same time, the gate signal line 17a(7) is selected (Vgl voltage) and a programming current flows through the source signal line 18 in the direction from the transistor 11a in the selected pixel row (7) to the source driver circuit 14. Through this operation, regular image data is held in the pixel row (2). The entire screen is redrawn as it is scanned by shifting pixel rows one by one through the above operations.

With the drive method in Figure 20, since each pixel is programmed with a twice larger current, ideally the emission brightness of the EL element 15 of each pixel is two times higher. Thus, the brightness of the display screen is twice higher than a predetermined value. To equalize this

brightness with the predetermined brightness, an area which includes the write pixel rows 51 and which is half as large as the display screen 50 can be turned into a non-display area 52 as illustrated in figure 16.

As is the case with Figure 13, when one display area 53 moves from top to bottom of the screen as shown in figure 20, the movement of the display area 53 is recognized visually if a low frame rate is used. It tends to be recognized easily especially when the user closes his/her eyes or moves his/her head up and down.

To deal with this problem, the display area 53 can be divided into a plurality of parts as illustrated in Figure 22. If the total area of the divided non-display area 52 is $S (N - 1)/N$, the brightness is equal to the brightness of the undivided display area.

Figure 23 shows voltage waveforms applied to gate signal lines 17. Figure 21 differs from Figure 23 basically in the operation of the gate signal line 17b. The gate signal line 17b is turned on and off (Vgl and Vgh) as many times as there are screen divisions. Figure 23 is the same as Figure 21 in other respects, and thus description thereof will be omitted.

As described above, dividing the display area 53 reduces flickering of the screen. Thus, a flicker-free good image display can be achieved. Incidentally, the display area 53 may be divided more finely. The more finely the display area

53 is divided, the less flickering occurs. Since the EL element 15 is highly responsive, even if it is turned on and off at intervals shorter than 5 μsec, there is no lowering of the display brightness.

With the drive method according to the present invention, the EL element 15 can be turned on and off by turning on and off a signal applied to the gate signal line 17b. Thus, the drive method according to the present invention can perform control using a low frequency on the order of KHz. Also, it does not need an image memory or the like in order to insert a black screen (insert a non-display area 52). Thus, the drive circuit or method according to the present invention can be implemented at low costs.

Figure 24 shows a case in which two pixel rows are selected simultaneously. It was found that on a display panel formed by low-temperature polysilicon technology, a method in which two pixel rows were selected simultaneously provided uniform display on a practical level. Probably this is because driver transistors 11a in adjacent pixels had very similar characteristics. In laser annealing, good results were obtained when laser stripes were irradiated in parallel with the source signal line 18.

This is because that part of a semiconductor film which is annealed simultaneously has uniform characteristics. That is, the semiconductor film is created uniformly within an

irradiation range of laser stripes and the Vt and mobility
of the transistors which use the semiconductor film are almost
uniform. Thus, if a striped laser shot is moved in parallel
with the source signal line 18, pixels (a pixel column, i.e.,
pixels arranged vertically on the screen) along the source
signal line 18 take on almost equal characteristics.
Therefore, if a plurality of pixel rows are turned on
simultaneously for current programming, the current obtained
by dividing the programming current by the number of selected
pixels are programmed almost uniformly into the pixels This
makes it possible to program a current close to a target value
and achieve uniform display. Thus, the direction of a laser
shot and the drive method described with reference to Figure
24 and the like have a synergistic effect.

As described above, if the direction of a laser shot is
made to coincide approximately with the direction of the source
signal line 18 (see Figure 7), the characteristics of the pixel
transistors 11a arranged vertically become almost uniform,
making it possible to do proper current programming (even if
the characteristics of the pixel transistors 11a arranged
horizontally are not uniform). The above operation is
performed in sync with 1 H (one horizontal scanning period)
by shifting selected pixel rows one by one or by shifting two
or more selected pixel rows at once.

Incidentally, as described with reference to Figure 8, the direction of the laser shot does not always need to be parallel with the direction of the source signal line 18. This is because even if the laser shot is directed at angles to the source signal line 18, pixel transistors 11a placed along one source signal line 18 can be made to take on almost equal characteristics. Thus, directing a laser shot in parallel with the source signal line 18 means bringing a pixel vertically adjacent to an arbitrary pixel along the source signal line 18 into a laser irradiation range. Besides, a source signal line 18 generally constitutes wiring which transmits programming current or voltage used as a video signal.

Incidentally, in the examples of the present invention a write pixel row is shifted every 1 H, but this is not restrictive. Pixel rows may be shifted every 2 Hs (two pixel rows at a time). Also, more than two pixel rows may be shifted at a time. Also, pixel rows may be shifted at desired time intervals or every second pixel may be shifted.

The shifting interval may be varied according to locations on the screen. For example, the shifting interval may be decreased in the middle of the screen, and increased at the top and bottom of the screen. For example, a pixel row may be shifted at intervals of 200 μsec. in the middle of the screen 50, and at intervals of 100 μsec. at the top and bottom of the screen 50. This increases emission brightness in the

middle of the screen 50 and decreases it around the perimeters (at the top and bottom of the screen 50)). Needless to say, the shifting interval is varied smoothly among the top, middle, and bottom of the screen 50 to avoid brightness contours.

Incidentally, the reference voltage of the source driver circuit 14 may be varied with the scanning location on the screen 50 (see Figure 146, etc.). For example, a reference current of 10 µA is used in the middle of the screen 50 and a reference current of 5 µA is used at the top of the screen 50. Varying a reference current in this way corresponding to a location in the screen 50, increases emission brightness in the middle of the screen 50 and decreases it around the perimeters (at the top and bottom of the screen 50)). Needless to say, the reference current is varied smoothly among the top, middle, and bottom of the screen 50 to avoid brightness contours.

Also, it goes without saying that images may be displayed by combining a drive method which varies the pixel-row shifting interval with the location on the screen and a drive method which varies the reference voltage with the location on the screen 50.

The shifting interval may be varied on a frame-by-frame basis. Also, it is not strictly necessary to select consecutive pixel rows. For example, every second pixel row may be selected.

Specifically, a possible drive method involves selecting the first and third pixel rows in the first horizontal scanning period, the second and fourth pixel rows in the second horizontal scanning period, the third and fifth pixel rows in the third horizontal scanning period, and the fourth and sixth pixel rows in the fourth horizontal scanning period. Of course, a drive method which involves selecting the first, third, and fifth pixel rows in the first horizontal scanning period also belongs to the technical category of the present invention. Also, one in every few pixel rows may be selected.

Incidentally, the combination of the direction of a laser shot and selection of multiple pixel rows is not limited to the pixel configurations in Figures 1, 2, and 32, but it is also applicable to other current-driven pixel configurations such as the current-mirror pixel configurations in Figures 38, 42, 50, etc. Also, it can be applied to voltage-driven pixel configurations in Figures 43, 51, 54, 62, etc. This is because as long as transistors in upper and lower parts of the pixel have equal characteristics, current programming can be performed properly using the voltage value applied to the same source signal line 18.

In Figure 24, when the write pixel row is the (1)-th pixel row, the gate signal lines 17a(1) and (2) are selected (see Figure 25). That is, the switching transistors 11b and the transistors 11c in the pixel rows (1) and (2) are on. Thus,

at least the switching transistors 11d in the pixel rows (1) and (2) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52. Incidentally, in Figure 24, the display area 53 is divided into five parts to reduce flickering.

Ideally, the transistors 11a in the two pixel rows deliver a current of Iw × 5 each to the source signal line 18 (when N = 10. Since K = 2, a current of Iw × K × 5 = Iw × 10 flows through the source signal line 18). Then, the capacitor 19 of each pixel 16 is programmed with a 5 times larger current.

Since two pixel rows are selected simultaneously (K = 2), two driver transistors 11a operate. That is, 10/2 = 5 times larger current flows through the transistor 11a per pixel. The total programming current of the two transistors 11a flows through the source signal line 18.

For example, if the current written into the write pixel row 51a is Id, a current of Iw × 10 is passed through the source signal line 18. There is no problem because regular image data is written into the write pixel row 51b later. The pixel row 51b provides the same display as the pixel row 51a during a period of 1 H. Consequently, at least the write pixel row 51a and the pixel row 51b selected to increase current are in non-display mode 52.

After the next 1 H, the gate signal line 17a(1) becomes deselected and a turn-on voltage (Vg1) is applied to the gate signal line 17b. At the same time, the gate signal line 17a(3) is selected (Vg1 voltage) and a programming current flows through the source signal line 18 in the direction from the transistor 11a in the selected pixel row (3) to the source driver circuit 14. Through this operation, regular image data is held in the pixel row (1).

After the next 1 H, the gate signal line 17a(2) becomes deselected and a turn-on voltage (Vg1) is applied to the gate signal line 17b. At the same time, the gate signal line 17a(4) is selected (Vg1 voltage) and a programming current flows through the source signal line 18 in the direction from the transistor 11a in the selected pixel row (4) to the source driver circuit 14. Through this operation, regular image data is held in the pixel row (2). The entire screen is redrawn as it is scanned by shifting pixel rows one by one through the above operations (of course, two or more pixel rows may be shifted simultaneously. For example, in the case of pseudo-interlaced driving, two pixel rows will be shifted at a time. Also, from the viewpoint of image display, the same image may be written into two or more pixel rows).

As in the case of Figure 16, with the drive method in Figure 24, since each pixel is programmed with a five times larger current (voltage), ideally the emission brightness of

the EL element 15 is five times higher. Thus, the brightness
of the display area 53 is five times higher than a predetermined
value. To equalize this brightness with the predetermined
brightness, an area which includes the write pixel rows 51
and which is 1/5 the display screen 50 can be turned into a
non-display area 52.

As shown in Figure 27, two write pixel rows 51 (51a and
51b) are selected in sequence from the upper side to the lower
side of the screen 50 (see also Figure 26. Pixels 16a and
16b are selected in Figure 26). However, at the bottom of
the screen, there does not exist 51b although the write pixel
row 51a exists as shown in Figure 27 (b). That is, there is
only one pixel row to be selected. Thus, the current applied
to the source signal line 18 is all written into the write
pixel row 51a. Consequently, twice as large a current as usual
is written into the write pixel row 51a.

To deal with this problem, the present invention forms
(places) a dummy pixel row 281 at the bottom of the screen
50, as shown in Figure 27(b). Thus, after the pixel row at
the bottom of the screen 50 is selected, the final pixel row
of the screen 50 and the dummy pixel row 281 are selected.
Consequently, a prescribed current is written into the write
pixel row in Figure 27(b).

Incidentally, although the dummy pixel row 281 is
illustrated as being adjacent to the top end or bottom end

of the display screen 50, this is not restrictive. It may be formed at a location away from the display screen 50. Besides, the dummy pixel row 281 does not need to contain a switching transistor 11d or EL element 15 such as those shown in Figure 1. This reduces the size of the dummy pixel row 281.

Figure 28 shows a mechanism of how the state shown in Figure 27(b) takes place. As can be seen from Figure 28, after the pixel 16c at the bottom of the screen 50 is selected, the final pixel row (dummy pixel row) 281 of the screen 50 is selected. The dummy pixel row 281 is placed outside the screen 50. That is, the dummy pixel row (dummy pixel) 281 does not illuminate, is not illuminated, or is hidden even if illuminated. For example, contact holes between the pixel electrode 105 and transistor 11 are eliminated, no EL film is formed on the dummy pixel row 281, or the like. Also, an insulating film may be formed on the pixel electrode 105 of the dummy pixel row 271.

Although it has been stated with reference to Figure 27 that the dummy pixel (row) 281 is provided (formed or placed) at the bottom of the screen 50, this is not restrictive. For example when the screen is scanned from bottom to top (inverse scanning) as shown in Figure 29(a), a dummy pixel row 281 should also be formed at the top of the screen 50 as shown in Figure 29(b). That is, dummy pixel rows 281 are formed (placed) both at the top and bottom of the screen 50. This configuration

accommodates inverse scanning of the screen as well. Two pixel rows are selected simultaneously in the example described above.

The present invention is not limited to this. For example, five pixel rows may be selected simultaneously (see Figure 23). When five pixel rows are selected simultaneously, four dummy pixel rows 281 should be formed. That is, the number of dummy pixel rows 281 equals the number of pixel rows selected simultaneously minus one. However, this is true only when the selected pixel rows are shifted one by one. When two or more pixel rows are shifted at a time, $(M - 1) \times L$ dummy pixel rows should be formed, where M is the number of pixels selected and L is the number of pixel rows shifted at a time.

The dummy pixel row configuration or dummy pixel row driving according to the present invention uses one or more dummy pixel rows. Of course, it is preferable to use the dummy pixel row driving and N-fold pulse driving in combination.

In the drive method which selects two or more pixel rows at a time, the larger the number of pixel rows selected simultaneously, the more difficult it becomes to absorb variations in the characteristics of the transistors 11a. However, the current programmed into one pixel increases with decreases in the number M of pixel rows selected simultaneously, resulting in a large current flowing through the EL element 15, which in turn makes the EL element 15 prone to degradation.

Figure 30 shows how to solve this problem. The basic concept behind Figure 30 is to use a method of selecting a plurality of pixel rows simultaneously during 1/2 H (1/2 of a horizontal scanning period) as described with reference to Figures 22 and 29 and to use a method of selecting one pixel row in the latter 1/2 H (1/2 of the horizontal scanning period) as described with reference to Figures 5 and 13. This combination makes it possible to absorb variations in the characteristics of the transistors 11a and achieve high speed and uniform surfaces. Incidentally, although the period of 1/2 H is used for ease of understanding, this is not restrictive. The first period may be 1/4 H and the second period may be 3/4 H.

Referring to Figure 30, for ease of understanding, it is assumed that five pixel rows are selected simultaneously in the first period and that one pixel row is selected in the second period. First, as shown in Figure 30(a1), in the first period (first 1/2 H), five pixel rows are selected simultaneously. This operation has been described with reference to Figure 22, and thus description thereof will be omitted. As an example, it is assumed that the current passed through the source signal line 18 is 25 times as large as a predetermined value. Thus, the transistor 11a in the pixel 16 (in the pixel configuration in Figure 1) is programmed with a five times larger current (25/5 pixel rows = 5). Since the

current is 25 times larger, the parasitic capacitance generated in the source signal line 18 and the like is charged and discharged in an extremely short period. Consequently, the potential of the source signal line 18 reaches a target potential in a short period of time and the terminal voltage of the capacitor 19 of each pixel 16 is programmed to pass a 25 times larger current. The 25 times larger current is applied in the first 1/2 H (1/2 of the horizontal scanning period).

Naturally, since the same image data is written into the five write pixel rows, the transistors 11d in the five write pixel rows are turned off in order not to display the image. Thus, the display condition is as shown in Figure 30(a2).

In the next 1/2 H period, one pixel is selected for current (voltage) programming. The condition is as shown in Figure 30(b1). Current (voltage) programming is performed so as to pass a five times larger current through the write pixel row 51a as in the first period. Equal current is passed in Figure 30(a1) and Figure 30(b1) to reach a target current more quickly by decreasing the changes in the terminal voltage of the programmed capacitor 19.

Specifically, in Figure 30(a1), current is passed through a plurality of pixels, approaching an approximate target value quickly. In this first stage, since a plurality of transistors 11a are programmed, variations in the transistors cause error

with respect to the target value. In the second stage, only a pixel row where data will be written and held is selected and complete programming is performed by changing the value of current from the approximate target value to a predetermined target value.

Incidentally, scanning of the non-illuminated area 52 from top to bottom of the screen and scanning of the write pixel rows 51a from top to bottom of the screen are performed in the same manner as in examples in Figure 13 and the like, and thus description thereof will be omitted.

Figure 31 shows drive waveforms used to implement the drive method shown in Figure 30. As can be seen from Figure 31, 1 H (one horizontal scanning period) consists of two phases. An ISEL signal is used to switch between the two phases. The ISEL signal is illustrated in Figure 31.

First, the ISEL signal will be described. The driver circuit 14 which performs operations shown in Figure 30 comprises a current output circuit A and current output circuit B. Each of the current output circuits consists of a D/A circuit which converts 8-bit gradation data from digital to analog, an operation amplifier, etc. In the example in Figure 30, the current output circuit A is configured to output 25 times larger current. On the other hand, the current output circuit B is configured to output 5 times larger current. Outputs from the current output circuit A and current output

circuit B are controlled by a switch circuit formed (placed) in a current output section through the ISEL signals and are applied to the source signal line 18. Such current output circuits are placed on each source signal line 18.

When the ISEL signal is low, the current output circuit A which outputs 25 times larger current is selected and current from the source signal line 18 is absorbed by the source driver IC 14 (more precisely, the current is absorbed by the current output circuit A formed in the source driver IC 14). The magnification (such as x25 or x5) of the current from the current output circuits can be adjusted easily using a plurality of resisters and an analog switch.

As shown in Figure 30, when the write pixel row is the (1)-th pixel row (see the 1H column in Figure 30), the gate signal lines 17a(1), (2), (3), (4), and (5) are selected (in the case of configuration shown in Figure 1). That is, the switching transistors 11b and the transistors 11c in the pixel rows (1), (2), (3), (4), and (5) are on. Besides, since ISEL is low, the current output circuit A which outputs 25 times larger current is selected and connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b. Thus, the switching transistors 11d in the pixel rows (1), (2), (3), (4), and (5) are off and current does not flow through the EL elements 15 in the corresponding

pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Ideally, the transistors 11a in the five pixels deliver a current of Iw × 2 each to the source signal line 18. Then, the capacitor 19 of each pixel 16 is programmed with a five times larger current. For ease of understanding, it is assumed here that the transistors have equal characteristics (Vt and S value).

Since five pixel rows are selected simultaneously (K = 5), five driver transistors 11a operate. That is, 25/5 = 5 times larger current flows through the transistor 11a per pixel. The total programming current of the five transistors 11a flows through the source signal line 18. For example, if the current written into the write pixel row 51a by a conventional drive method is Iw, a current of Iw × 25 is passed through the source signal line 18. The write pixel rows 51b into which image data is written later than the write pixel row (1) are auxiliary pixel rows used to increase the amount of current delivered to the source signal line 18. However, there is no problem because regular image data is written into the write pixel rows 51b later.

Thus, the pixel rows 51b provide the same display as the pixel row 51a during a period of 1 H. Consequently, at least the write pixel row 51a and the pixel rows 51b selected to increase current are in non-display mode 52.

In the next 1/2 H period (1/2 of the horizontal scanning period), only the write pixel row 51a is selected. That is, only the (1)-th pixel row is selected. As can be seen from Figure 31, a turn-on voltage (Vgl) is applied only to the gate signal line 17a(1) and a turn-off voltage (Vgh) is applied to the gate signal lines 17a(2), (3), (4), and (5). Thus, the transistor 11a in the pixel row (1) is in operation (supplying current to the source signal line 18), but the switching transistors 11b and the transistors 11c in the pixel rows (2), (3), (4), and (5) are off. That is, they are non-selected.

Besides, since ISEL is high, the current output circuit B which outputs 5 times larger current is selected and connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b, which is in the same state as during the first 1/2 H. Thus, the switching transistors 11d in the pixel rows (1), (2), (3), (4), and (5) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Thus, each transistor 11a in the pixel row (1) deliver a current of Iw × 5 to the source signal line 18. Then, the capacitor 19 in each pixel row (1) is programmed with a 5 times larger current.

In the next horizontal scanning period, the write pixel row shifts by one. That is, the pixel row (2) becomes the current write pixel row. During the first 1/2 H period, when the write pixel row is the (2)-th pixel row, the gate signal lines 17a(2), (3), (4), and (5) and (6) are selected. That is, the switching transistors 11b and the transistors 11c in the pixel rows (2), (3), (4), (5), and (6) are on. Besides, since ISEL is low, the current output circuit A which outputs 25 times larger current is selected and connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b.

Thus, the switching transistors 11d in the pixel rows (2), (3), (4), (5), and (6) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52. On the other hand, since Vgl voltage is applied to the gate signal line 17b(1) of the pixel row (1), the transistor 11d is on and the EL element 15 in the pixel row (1) illuminates.

Since five pixel rows are selected simultaneously (K = 5), five driver transistors 11a operate. That is, 25/5 = 5 times larger current flows through the transistor 11a per pixel. The total programming current of the five transistors 11a flows through the source signal line 18.

In the next 1/2 H period (1/2 of the horizontal scanning period), only the write pixel row 51a is selected. That is,

only the (2)-th pixel row is selected. As can be seen from Figure 31, a turn-on voltage (Vgl) is applied only to the gate signal line 17a(2) and a turn-off voltage (Vgh) is applied to the gate signal lines 17a (3), (4), (5), and (6).

Thus, the transistors 11a in the pixel rows (1) and (2) are in operation (the pixel row (1) supplies current to the EL element 15 and the pixel row (2) supplies current to the source signal line 18), but the switching transistors 11b and the transistors 11c in the pixel rows (3), (4), (5), and (6) are off. That is, they are non-selected.

Besides, since ISEL is high, the current output circuit B which outputs 5 times larger current is selected and the current output circuit 1222b is connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b, which is in the same state as during the first 1/2 H. Thus, the switching transistors 11d in the pixel rows (2), (3), (4), (5), and (6) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Thus, each transistor 11a in the pixel row (1) deliver a current of Iw × 5 to the source signal line 18. Then, the capacitor 19 in each pixel row (1) is programmed with a 5 times larger current. The entire screen is drawn as the above operations are performed in sequence.

The drive method described with reference to Figure 30 selects G pixel rows (G is 2 or larger) in the first period and does programming in such a way as to pass N times larger current through each pixel row. In the second period, the drive method selects B pixel rows (B is smaller than G, but not smaller than 1) and does programming in such a way as to pass an N times larger current through the pixels.

Another scheme is also available. It selects G pixel rows (G is 2 or larger) in the first period and does programming in such a way that the total current in all the pixel rows will be an N times larger current. In the second period, this scheme selects B pixel rows (B is smaller than G, but not smaller than 1) and does programming in such a way that the total current in the selected pixel rows (the current in the one pixel row if one pixel row is selected) will be an N times larger current. For example, in Figure 30(a1), five pixel rows are selected simultaneously and a twice larger current is passed through the transistor 11a in each pixel. Thus, $5 \times 2 = 10$ times larger current flows through the source signal line 18. In the second period, one pixel row is selected in Figure 30(b1). A 10 times larger current is passed through the transistor 11a in this pixel.

Incidentally, although a plurality of pixel rows are selected simultaneously in a period of 1/2 H and a single pixel row is selected in a period of 1/2 H in Figure 31, this is

not restrictive. A plurality of pixel rows may be selected simultaneously in a period of 1/4 H and a single pixel row may be selected in a period of 3/4 H. Also, the sum of the period in which a plurality of pixel rows are selected simultaneously and the period in which a single pixel row is selected is not limited to 1 H. For example, the total period may be 2 Hs or 1.5 Hs.

In Figure 30, it is also possible to select two pixel rows simultaneously in the second period after selecting five pixel rows simultaneously in the first 1/2 H. This can also achieve a practically acceptable image display.

In Figure 30, pixel rows are selected in two stages--five pixel rows are selected simultaneously in the first 1/2 H period and a single pixel row is selected in the second 1/2 H period, but this is not restrictive. For example, it is also possible to select five pixel rows simultaneously in the first stage, select two of the five pixel rows in the second stage, and finally select one pixel row in the third stage. In short, image data may be written into pixel rows in two or more stages.

In the example described above, pixel rows are selected one by one and programmed with current, or two or more pixel rows are selected at a time and programmed with current. However, the present invention is not limited to this. It is also possible to use a combination of the two methods according to image data: the method of selecting pixel rows

one by one and programming them with current and the method
of selecting two or more pixel rows at a time and programming
them with current.

Figure 186 combines a drive system which selects pixel
rows one by one and a drive method which selects multiple pixel
rows one by one.
In the case where multiple pixel rows are selected at a time,
it is assumed for ease of understanding that two pixel rows
are selected simultaneously as illustrated in Figure 186(a2).
Thus, one dummy pixel row 281 each is formed at the top and
bottom of the screen.
The drive system which selects pixel rows one by one does not
need to use dummy pixel rows.

Incidentally, for ease of understanding, it is assumed
that the source driver IC 14 in Figure 186(a1) (one pixel row
is selected) and Figure 186(a2) (two pixel rows are selected)
output equal currents.
Thus, the drive system which selects two pixel rows at a time
as shown in Figure 186(a2) provides half the screen brightness
compared to the drive system which selects pixel rows one by
one as shown in Figure 186(a1).
To provide equal screen brightness, the duty ratio in Figure
186(a2) can be doubled (e.g., if the duty ratio in Figure 186(a1)
is 1/2, the duty ratio in Figure 186(a2) can be set to 1/1
= 1/2 × 2).

Also, the magnitude of the reference current inputted in the source driver IC 14 can be varied twice as much. Alternatively, the programming current can be doubled.

Figure 186(a1) shows a typical drive method according to the present invention.

If input video signals are non-interlaced (progressive) signals, the drive system in Figure 186(a1) is used.

If input video signals are interlaced signals, the drive system in Figure 186(a2) is used.

Also, if video signals have low image resolution, the drive system in Figure 186(a2) is used.

It is also possible to use the drive method in Figure 186(a2) for moving pictures and the drive method in Figure 186(a1) for still pictures.

The drive method in Figure 186(a1) and drive method in Figure 186(a2) can be switched easily by controlling the start pulse supplied to the gate driver circuit 12.

A problem is that the drive system which selects two pixel rows at a time as shown in Figure 186(a2) provides half the screen brightness compared to the drive system which selects pixel rows one by one (Figure 186(a1)).

To provide equal screen brightness, the duty ratio in Figure 186(a2) can be doubled (e.g., if the duty ratio in Figure 186(a1) is 1/2, the duty ratio in Figure 186(a2) can be set to 1/1 = 1/2 × 2).

That is, the proportions of the non-display area 52 and display area 53 in Figure 186(b) can be varied.

The proportions of the non-display area 52 and display area 53 in Figure 186(b) can be varied easily by controlling the start pulse supplied to the gate driver circuit 12. That is, the drive mode in Figure 186(b) can be varied according the display mode in Figures 186(a1) and 186(a2).

Now, interlaced driving according to the present invention will be described below in more detail. Figure 187 shows a configuration of the display panel according to the present invention which performs the interlaced driving. In Figure 187, the gate signal lines 17a of odd-numbered pixel rows are connected to a gate driver circuit 12a1. The gate signal lines 17a of even-numbered pixel rows are connected to a gate driver circuit 12a2. On the other hand, the gate signal lines 17b of the odd-numbered pixel rows are connected to a gate driver circuit 12b1. The gate signal lines 17b of the even-numbered pixel rows are connected to a gate driver circuit 12b2.

Thus, through operation (control) of the gate driver circuit 12a1, image data in the odd-numbered pixel rows are rewritten in sequence. In the odd-numbered pixel rows, illumination and non-illumination of the EL elements are controlled through operation (control) of the gate driver circuit 12b1. Also, through operation (control) of the gate

driver circuit 12a2, image data in the even-numbered pixel rows are rewritten in sequence. In the even-numbered pixel rows, illumination and non-illumination of the EL elements are controlled through operation (control) of the gate driver circuit 12b2.

Figure 188(a) shows operating state in the first field of the display panel. Figure 188(b) shows operating state in the second field of the display panel. In Figure 188, the oblique hatching which marks the gate driver circuits 12 indicates that the gate driver circuits 12 are not taking part in data scanning operation. Specifically, in the first field in Figure 188(a), the gate driver circuit 12a1 is operating for write control of programming current and the gate driver circuit 12b2 is operating for illumination control of the EL element 15. In the second field in Figure 188(b), the gate driver circuit 12a2 is operating for write control of programming current and the gate driver circuit 12b1 is operating for illumination control of the EL element 15. The above operations are repeated within the frame.

Figure 189 shows image display status in the first field. Figure 189(a) illustrates write pixel rows (locations of odd-numbered pixel rows programmed with current (voltage). The location of the write pixel row is shifted in sequence: Figure 189(a1) → (a2) → (a3). In the first field, odd-numbered pixel rows are rewritten in sequence (image data

in the even-numbered pixel rows are maintained). Figure 189(b) illustrates display status of odd-numbered pixel rows. Incidentally, Figure 189(b) illustrates only odd-numbered pixel rows. Even-numbered pixel rows are illustrated in Figure 189(c). As can be seen from Figure 189(b), the EL elements 15 of the pixels in the odd-numbered pixel rows are non-illuminated. On the other hand, the even-numbered pixel rows are scanned in both display area 53 and non-display area 52 as shown in Figure 189(c) (N-fold pulse driving).

Figure 190 shows image display status in the second field. Figure 190(a) illustrates write pixel rows (locations of odd-numbered pixel rows programmed with current (voltage). The location of the write pixel row is shifted in sequence: Figure 190(a1) → (a2) → (a3). In the second field, even-numbered pixel rows are rewritten in sequence (image data in the odd-numbered pixel rows are maintained). Figure 190(b) illustrates display status of odd-numbered pixel rows. Incidentally, Figure 190(b) illustrates only odd-numbered pixel rows. Even-numbered pixel rows are illustrated in Figure 190(c). As can be seen from Figure 190(b), the EL elements 15 of the pixels in the even-numbered pixel rows are non-illuminated. On the other hand, the odd-numbered pixel rows are scanned in both display area 53 and non-display area 52 as shown in Figure 190(c) (N-fold pulse driving).

In this way, interlaced driving can be implemented easily on an EL display panel. Also, N-fold pulse driving eliminates shortages of write current and blurred moving pictures. Besides, current (voltage) programming and illumination of EL elements 15 can be controlled easily and circuits can be implemented easily.

Incidentally, the drive method according to the present invention is not limited to those shown in Figures 189 and 190. For example, a drive method shown in Figure 191 is also available. Whereas in Figures 189 and 190, the odd-numbered pixel rows or even-numbered pixel rows being programmed belong to a non-display area 52 (non-illumination or black display), the example in Figure 191 involves synchronizing the gate driver circuits 12b1 and 12b2 which control illumination of the EL elements 15. Needless to say, however, the write pixel row 51 being programmed with current (voltage) belongs to a non-display area (there is no need for this in the case of the current-mirror pixel configuration in Figure 38). In Figure 191, since illumination control is common to the odd-numbered pixel rows and even-numbered pixel rows, there is no need to provide two gate driver circuits: 12b1 and 12b2. The gate driver circuit 12b alone can perform illumination control.

The drive method in Figure 191 uses illumination control for both odd-numbered pixel rows and even-numbered pixel rows.

However, the present invention is not limited to this. Figure 192 shows an example in which illumination control varies between odd-numbered pixel rows and even-numbered pixel rows. In Figure 192, the illumination mode (display area 53 and non-display area 52) of odd-numbered pixel rows and illumination mode of even-numbered pixel rows have opposite patterns. Thus, display area 53 and non-display area 52 have the same size. However, this is not restrictive.

In the above example, the drive method programs pixel rows with current (voltage) one at a time. However, the drive method according to the present invention is not limited to this. Needless to say, two pixel rows (a plurality of pixel rows) may be programmed with current (voltage) simultaneously as shown in Figure 193.

Besides, in Figures 190 and 189, it is not strictly necessary to put all the odd-numbered pixel rows or even-numbered pixel rows in non-illumination mode.

The N-fold pulse driving method according to the present invention uses the same waveform for the gate signal lines 17b of different pixel rows and applies current by shifting the pixel rows at 1 H intervals. The use of such scanning makes it possible to shift illuminating pixel rows in sequence with the illumination duration of the EL elements 15 fixed to 1F/N. It is easy to shift pixel rows in this way while using the same waveform for the gate signal lines 17b of the

pixel rows. It can be done by simply controlling data ST1 and ST2 applied to the shift register circuits 61a and 61b in Figure 6. For example, if Vg1 is output to the gate signal line 17b when input ST1 is low and Vgh is output to the gate signal line 17b when input ST1 is high, ST2 applied to the shift register circuit 17b can be set low for a period of 1F/N and set high for the remaining period. Then, inputted ST2 can be shifted using a clock CLK2 synchronized with 1 H.

Incidentally, the EL elements 15 must be turned on and off at intervals of 0.5 msec or longer. Short intervals will lead to insufficient black display due to persistence of vision, resulting in blurred images and making it look as if the resolution has lowered. This also represents a display state of a data holding display. However, increasing the on/off intervals to 100 msec will cause flickering. Thus, the on/off intervals of the EL elements must be not shorter than 0.5 μsec and not longer than 100 msec. More preferably, the on/off intervals should be from 2 msec to 30 msec (both inclusive). Even more preferably, the on/off intervals should be from 3 msec to 20 msec (both inclusive).

As also described above, an undivided black screen 152 achieves good movie display, but makes flickering of the screen more noticeable. Thus, it is desirable to divide the black insert into multiple parts. However, too many divisions will cause moving pictures to blur. The number of divisions should

be from 1 to 8 (both inclusive). More preferably, it should

be from 1 to 5 (both inclusive).

Incidentally, it is preferable that the number of

divisions of a black screen can be varied between still pictures

and moving pictures. When N = 4, 75% is occupied by a black

screen and 25% is occupied by image display. When the number

of divisions is 1, a strip of black display which makes up

75% is scanned vertically. When the number of divisions is

3, three blocks are scanned, where each block consists of a

black screen which makes up 25% and a display screen which

makes up 25/3 percent. The number of divisions is increased

for still pictures and decreased for moving pictures. The

switching can be done either automatically according to input

images (detection of moving pictures) or manually by the user.

Alternatively, the switching can be done according to input

outlet such as video on the display apparatus.

For example, for wallpaper display or an input screen

on a cell phone, the number of divisions should be 10 or more

(in extreme cases, the display may be turned on and off every

1 H). When displaying moving pictures in NTSC format, the

number of divisions should be from 1 to 5 (both inclusive).

Preferably, the number of divisions can be switched in three

or more steps; for example, 0, 2, 4, 8 divisions, and so on

Preferably, the ratio of the black screen to the entire

display screen should be from 0.2 to 0.9 (from 1.2 to 9 in

terms of N) both inclusive when the area of the entire screen

is taken as 1. More preferably, the ratio should be from 0.25

to 0.6 (from 1.25 to 6 in terms of N) both inclusive. If the

ratio is 0.20 or less, movie display is not improved much.

When the ratio is 0.9 or more, the display part becomes bright

and its vertical movements become liable to be recognized

visually.

Also, preferably, the number of frames per second is from

10 to 100 (10 Hz to 100 Hz) both inclusive. More preferably,

it is from 12 to 65 (12 Hz to 65 Hz) both inclusive. When

the number of frames is small, flickering of the screen becomes

conspicuous while too large a number of frames makes writing

from the source driver circuit 14 and the like difficult,

resulting in deterioration of resolution.

The present invention allows the brightness of images

to be varied by controlling the gate signal lines 17.

However, needless to say, the brightness of images may be varied

by varying the current (voltage) applied to the source signal

lines 18. It goes without saying that the two methods described

above (Figures 33 and 35 and the like) may be used in combination:

the method of controlling the gate signal lines 17 and the

method of varying the current (voltage) applied to the source

signal lines 18.

Needless to say, the above items also apply to the pixel

configurations for current programming in Figure 38 and the

like as well as to the pixel configurations for voltage

programming in Figures 43, 51, 54, and the like. This can

be accomplished through on/off control of the transistor 11d

in Figure 38, transistor 11d in Figure 43, and transistor 11e

in Figure 51. In this way, by turning on and off the wiring

which delivers current to the EL elements 15, the N-fold pulse

driving according to the present invention can be implemented

easily.

Also, the gate signal line 17b may be set to Vg1 for a

period of 1F/N anytime during the period of 1F (not limited

to 1F. Any unit time will do). This is because a predetermined

brightness is obtained by turning off the EL element 15 for

a predetermined period out of a unit time. However, it is

preferable to set the gate signal line 17b to Vg1 and illuminate

the EL element 15 immediately after the current programming

period (1 H). This will reduce the effect of retention

characteristics of the capacitor 19 in Figure 1.

Also, preferably the number of screen divisions is

configured to be variable. For example, when the user presses

a brightness adjustment switch or turns a brightness adjustment

knob, the value of K may be changed in response. Alternatively,

the value of K may be changed manually or automatically

depending on images or data to be displayed.

In this way, the mechanism for changing the value of K

(the number of divisions of the image display part 53) can

be implemented easily. This can be achieved by simply making the time to change ST (when to set ST low during 1F) adjustable or variable.

Incidentally, although it has been stated with reference to Figure 16 and the like that a period (1F/N) during which the gate signal line 17b is set to Vg1 is divided into a plurality of parts (K parts) and that a period of 1F/(K·N) during which the gate signal line 17b is set to Vg1 repeats K times, this is not restrictive. A period of 1F/(K·N) may be repeated L (L ≠ K) times. In other words, the present invention displays the display screen 50 by controlling the period (time) during which current is passed through the EL element 15. Thus, the idea of repeating the 1F/(K·N) period L (L ≠ K) times is included in the technical idea of the present invention. Also, by varying the value of L, the brightness of the display screen 50 can be changed digitally. For example, there is a 50% change of brightness (contrast) between L = 2 and L = 3. The control described here is also applicable to other examples of the present invention (of course, it is applicable to what is described later herein). These are also included in the N-fold pulse driving according to the present invention.

The above examples involve placing (forming) the transistor 11d serving as a switching element between the EL element 15 and driver transistor 11a and turning on and off the screen 50 by controlling the transistor 11d. This drive

method eliminates shortages of write current in black display condition during current programming and thereby achieves proper resolution or black display. That is, in current programming, it is important to achieve proper black display. The drive method described next achieves proper black display by resetting the driver transistor 11a. This example will be described below with reference to Figure 32.

The pixel configuration in Figure 32 is basically the same as the one shown in Figure 1. With the pixel configuration in Figure 32, a programmed Iw current flows through the EL element 15, illuminating the EL element 15. By being programmed, the driver transistor 11a retains a capability to pass current. The drive system shown in Figure 32 resets (turns off) the transistor 11a using this capability to pass current. Hereinafter, this drive system will be referred to as reset driving.

To implement reset driving using the pixel configuration shown in Figure 1, the transistors 11b and 11c must be able to be switched on and off independently of each other. Specifically, as illustrated in Figure 32, it is necessary to be able to independently control the gate signal line 17a (gate signal line WR) used for on/off control of the transistor 11b and the gate signal line 17c (gate signal line EL) used for on/off control of the transistor 11c. The gate signal

lines 17a and 17c can be controlled using two independent shift registers 61 as illustrated in Figure 6.

Preferably, the drive voltage should be varied between the gate signal line 17a which drives the transistor 11b and the gate signal line 17b which drives the transistor 11d (when the pixel configuration in Figure 1 is used). The amplitude value (difference between turn-on voltage and turn-off voltage) of the gate signal line 17a should be smaller than the amplitude value of the gate signal line 17b.

Too large an amplitude value of the gate signal line 17 will increase penetration voltage between the gate signal line 17 and pixel 16, resulting in an insufficient black level. The amplitude of the gate signal line 17a can be controlled by controlling the time when the potential of the source signal line 18 is not applied (or is applied (during selection)) to the pixel 16. Since changes in the potential of the source signal line 18 are small, the amplitude value of the gate signal line 17a can be made small.

On the other hand, the gate signal line 17b is used for on/off control of EL. Thus, its amplitude value becomes large. For this, output voltage is varied between the shift register circuits 61a and 61b. If the pixel is constructed of P-channel transistors, approximately equal Vgh (turn-off voltage) is used for the shift register circuits 61a and 61b while Vgl (turn-on voltage) of the shift register circuit 61a is made

lower than Vgl (turn-on voltage) of the shift register circuit 61b.

Reset driving will be described below with reference to Figure 33. Figure 33 is a diagram illustrating a principle of reset driving. First, as illustrated in Figure 33(a), the transistors 11c and 11d are turned off and the transistor 11b is turned on. As a result, the drain (D) terminal and gate (G) terminal of the driver transistor 11a are short-circuited, allowing a current Ib to flow. Generally, the transistor 11a has been programmed with current in the previous field (frame). In this state, as the transistor 11d is turned off and the transistor 11b is turned on, the drive current Ib flows through the gate (G) terminal of the transistor 11a. Consequently, the gate (G) terminal and drain (D) terminal of the transistor 11a have the same potential, resetting the transistor 11a (to a state in which no current flows).

The reset mode (in which no current flows) of the transistor 11a is equivalent to a state in which an offset voltage is held in voltage offset canceling mode described with reference to Figure 51 and the like.
That is, in the state in Figure 33(a), the offset voltage is held between the terminals of the capacitor 19.
The offset voltage varies with the characteristics of the transistor 11a. Thus, in Figure 33(a), a state in which the transistor 11a does not pass current is maintained in the

capacitor 19 in each pixel (i.e., the transistor 11a passes a black display current close to zero).

Incidentally, before the operation in Figure 33(a), it is preferable to turn off the transistors 11b and 11c, turn on the transistor 11d, and pass current through the driver transistor 11a. Preferably, this operation should be completed in a minimum time. Otherwise, there is a fear that a current will flow through the EL element 15, illuminating the EL element 15, and thereby lowering display contrast. Preferably, the operating time here is from 0.1% to 10% of 1 H (one horizontal scanning period) both inclusive. More preferably, it is from 0.2% to 2% or from 0.2 μsec to 5 μsec (both inclusive). Also, this operation (the operation to be performed before the operation in Figure 33(a)) may be performed on all the pixels 16 of the screen at once. This operation will lower the drain (D) terminal voltage of the driver transistor 11a, making it possible to pass the current Ib smoothly in the state shown in Figure 33(a). Incidentally, the above items also apply to other reset driving according to the present invention.

As the operation time of Figure 33(a) becomes longer, a larger Ib current tends to flow, reducing the terminal voltage of the capacitor 19. Thus, the operation time of Figure 33(a) should be fixed. It has been shown experimentally and

analytically that preferably the operation time in Figure 33 (a) is from 1 H to 5 Hs (both inclusive).

Preferably, this period should be varied among R, G, and B pixels. This is because EL material varies among different colors and rising voltage varies among different EL materials. Optimum periods suitable for EL materials should be specified separately for the R, G, and B pixels. Although it has been stated that the period should be from 1 H to 5 Hs (both inclusive) in this example, it goes without saying that the period may be 5 Hs or longer in the case of a drive system which mainly concerns black insertion (writing of a black screen). Incidentally, the longer the period, the better the black display condition of pixels.

A state shown in Figure 33 (b) occurs during a period of 1 H to 5 Hs (both inclusive) after the state in Figure 33 (a). Figure 33 (b) shows a state in which the transistors 11c and 11b are on and the transistor 11d is off. This is a state in which current programming is being performed, as described earlier. Specifically, a programming current Iw is output (or absorbed) from the source driver circuit 14 and passed through the driver transistor 11a. The potential of the gate (G) terminal of the driver transistor 11a is set so that the programming current Iw flows (the set potential is held in the capacitor 19).

If the programming current Iw is 0 A, the transistor 11a is held in the state in Figure 33(a) in which it does not pass current, and thus a proper black display is achieved. Also, when performing current programming for white display in Figure 33(b), the current programming is started from offset voltage of completely black display even if there are variations in the characteristics of driver transistors in pixels. Thus, the time required to reach a target current value becomes uniform according to gradations. This eliminates gradation errors due to variations in the characteristics of the transistors 11a, making it possible to achieve proper image display.

After the programming in Figure 33(b), the transistors 11b and 11c are turned off in sequence and the transistor 11d is turned on to deliver the programming current Iw (= Ie) to the EL element 15 from the driver transistor 11a, and thereby illuminate the EL element 15. What is shown in Figure 33(c) has already been described with reference to Figure 1 and the like, and thus detailed description thereof will be omitted.

The drive system (reset driving) described with reference to Figure 33 consists of a first operation of disconnecting the driver transistor 11a from the EL element 15 (so that no current flows) and shorting between the drain (D) terminal and gate (G) terminal of the driver transistor (or between the source (S) terminal and gate (G) terminal, or generally

speaking, between two terminals including the gate (G) terminal of the driver transistor) and a second operation of programming the driver transistor with current (voltage) after the first operation. At least the second operation is performed after the first operation. Incidentally, for reset driving, the transistors 11b and 11c must be able to be controlled independently as shown in Figure 32.

In image display mode (if instantaneous changes can be observed), the pixel row to be programmed with current is reset (black display mode) and is programmed with current after 1 H (also in black display mode because the transistor 11d is off). Next, current is supplied to the EL element 15 and the pixel row illuminates at a predetermined brightness (at the programmed current). That is, the pixel row of black display moves from top to bottom of the screen and it should look as if the image were rewritten at the location where the pixel row passed by.

Incidentally, although it has been stated that current programming is performed 1 H after a reset, this period may be approximately 5 Hs or shorter. This is because it takes a relatively long time for the reset in Figure 33(a) to be completed. If this period is 5 Hs, five pixel rows will be displayed in black (six pixel rows including the pixel row going through current programming).

Also, the number of pixel rows which are reset at a time is not limited to one, and two or more pixel rows may be reset at a time. It is also possible to reset and scan two or more pixel rows at a time by overlapping some of them. For example, if four pixel rows are reset at a time, pixel rows (1), (2), (3), and (4) are reset in the first horizontal scanning period (1 unit), pixel rows (3), (4), (5), and (6) are reset in the second horizontal scanning period, pixel rows (5), (6), (7), and (8) are reset in the third horizontal scanning period, and pixel rows (7), (8), (9), and (10) are reset in the fourth horizontal scanning period. Incidentally the drive operations in Figures 33(b) and 33(c) are naturally carried out in sync with the drive operation in Figure 33(a).

Needless to say, the drive operation of Figures 33(b) and 33(c) may be performed after resetting all the pixels in the screen simultaneously or during scanning. Also, it goes without saying that pixel rows may be reset (at intervals of one or more pixel rows) in interlaced driving mode (scanning at intervals of one or more pixel rows). Also, pixel rows may be reset at random. The reset driving according to the present invention involves operating pixel rows (i.e., controlling the vertical direction of the screen). However, the concept of reset driving does not limit control directions to the pixel row direction. For example, it goes without saying

that reset driving may be performed in the direction of pixel columns.

Incidentally, the reset driving in Figure 33 can achieve better image display if combined with the N-fold pulse driving according to the present invention or with interlaced driving. Particularly, the configuration in Figure 22 can easily implement intermittent N/K-fold pulse driving (this driving method provides two or more illuminated areas in a screen and can be implemented easily by turning on and off the transistor 11d by controlling the gate signal line 17b: this has been described earlier), and thus can achieve proper image display without flickering.

Needless to say, more excellent image display can be achieved by combining with a reverse bias drive method, a precharge drive method, a penetration voltage drive method, or the like described later. Thus, it goes without saying that reset driving can be performed in combination with other examples according to the present invention.

Figure 34 is a block diagram of a display apparatus which implement reset driving. The gate driver circuit 12a controls the gate signal line 17a and gate signal line 17b in Figure 32. By the application of on/off voltages to the gate signal line 17a, the transistor 11b is turned on and off. Also, by the application of on/off voltages to the gate signal line 17b, the transistor 11d is turned on and off. The gate driver

circuit 12b controls the gate signal line 17c in Figure 32. By the application of on/off voltages to the gate signal line 17c, the transistor 11c is turned on and off.

Thus, the gate signal line 17a is controlled by the gate driver circuit 12a while the gate signal line 17c is controlled by the gate driver circuit 12b. This makes it possible to freely specify the time to turn on the transistor 11b and reset the driver transistor 11a as well as the time to turn on the transistor 111c and program the driver transistor 11a with current. Other parts of the configuration are the same as or similar to those described earlier, and thus description thereof will be omitted.

Figure 35 is a timing chart of reset driving. While a turn-on voltage is applied to the gate signal line 17a to turn on the transistor 11b and reset the driver transistor 11a, a turn-off voltage is applied to the gate signal line 17b to keep the transistor 11d off. This creates the state shown in Figure 32(a). A current Ib flows during this period.

Although in the timing chart shown in Figure 35, the reset time is 2 Hs (when a turn-on voltage is applied to the gate signal line 17a and the transistor 11b is turned on), this is not restrictive. The reset time may be longer than 2 Hs. If a reset can be performed very quickly, the reset time may be less than 1 H.

The duration of the reset period can be changed easily using a DATA (ST) pulse period inputted in the gate driver circuit 12. For example, if DATA inputted in an ST terminal is set high for a period of 2 Hs, the reset period outputted for each gate signal line 17a is 2 Hs. Similarly, if DATA inputted in the ST terminal is set high for a period of 5 Hs, the reset period outputted for each gate signal line 17a is 5 Hs.

After a reset period of 1 H, a turn-on voltage is applied to the gate signal line 17c(1) of the pixel row (1). As the transistor 11c turns on, the programming current Iw applied to the source signal line 18 is written into the driver transistor 11a via the transistor 11c.

After current programming, a turn-off voltage is applied to the gate signal line 17c of the pixel row (1), the transistor 11c is turned off, and the pixel disconnected from the source signal line. At the same time, a turn-off voltage is also applied to the gate signal line 17a and the driver transistor 11a exits the reset mode (incidentally, the use of the term "current-programming mode" is more appropriate than the term "reset mode" to refer to this period). On the other hand, a turn-on voltage is applied to the gate signal line 17b, the transistor 11d is turned on, and the current programmed into the driver transistor 11a flows through the EL element 15. What has been said about the pixel row (1) similarly applies

to the pixel row (2) and subsequent pixel rows. Also, their operation is obvious from Figure 35. Thus, description of (2) and subsequent pixel rows will be omitted.

In Figure 35, the reset period has been 1 H. Figure 36 shows an example in which the reset period is 5 Hs. The duration of the reset period can be changed easily using the DATA (ST) pulse period inputted in the gate driver circuit 12. Figure 36 shows an example in which DATA inputted in the ST1 terminal of the gate driver circuit 12a is set high for a period of 5 Hs and the reset period outputted for each gate signal line 17a is 5 Hs. The longer the reset period, the more completely the reset is performed, resulting in a proper black display. However, display brightness is decreased accordingly.

In Figure 36, the reset period has been 5 Hs. Besides, the reset mode is continuous. However, the reset mode need not necessarily be continuous. For example, the signal outputted from each gate signal line 17a may be turned on and off every 1 H. Such on/off operation can be achieved easily by operating an enable circuit (not shown) formed in the output stage of the shift register or controlling the DATA (ST) pulses inputted in the gate driver circuit 12.

In the circuit configuration shown in Figure 34, the gate driver circuit 12a requires at least two shift register circuits (one for the gate signal line 17a, the other for the gate signal line 17b). This presents a problem of an increased

circuit scale of the gate driver circuit 12a.   Figure 37 shows

an example in which the gate driver circuit 12a has only one

shift register.   A timing chart of output signals resulting

from operation of the circuit in Figure 37 is shown in Figure

35.   Note that the gate signal lines 17 coming out of the gate

driver circuits 12a and 12b are denoted by different symbols

between Figures 35 and 37.

As can be seen from the fact that an OR circuit 371 is

included in Figure 37, the output of each gate signal line

17a is ORed with the output from the preceding stage to the

shift register circuit 61a.   That is, the gate signal line

17a outputs a turn-on voltage for a period of 2 Hs.   On the

other hand, the gate signal line 17c outputs the output of

the shift register circuit 61a as it is.   Thus, a turn-on

voltage is applied for a period of 1 H.

For example, if the shift register circuit 61a outputs

a high-level signal second, a turn-on voltage is output to

the gate signal lines 17c of the pixel 16(1), which now is

in a state of being programmed with current (voltage).   At

the same time, a turn-on voltage is also output to the gate

signal lines 17a of the pixel 16(2), turning on the transistor

11b of the pixel 16(2) and resetting the driver transistor

11a of the pixel 16(2).

Similarly, if the shift register circuit 61a outputs a

high-level signal third, a turn-on voltage is output to the

gate signal lines 17c of the pixel 16(2), which now is in a state of being programmed with current (voltage). At the same time, a turn-on voltage is also output to the gate signal lines 17a of the pixel 16(3, turning on the transistor 11b of the pixel 16(3) and resetting the driver transistor 11a of the pixel 16(3). Thus, the gate signal lines 17a outputs turn-on voltages for a period of 2 Hs, and the gate signal lines 17c receive a turn-on voltage for a period of 1 H.

In programming mode, since the transistors 11b and 11c turn on simultaneously (Figure 33(b)), if the transistor 11c turns off before the transistor 11b during transition to non-programming mode (Figure 33(c), the reset mode in Figure 33(b) occurs. To prevent this situation, the transistor 11c must be turned off after the transistor 11b. For that, a turn-on voltage needs to be applied to the gate signal line 17a earlier than the gate signal line 17c.

The above example concerns the pixel configuration in Figure 32 (basically, in Figure 1). However, the present invention is not limited to this. For example, it is also applicable to current-mirror pixel configurations such as the one shown in Figure 38. Incidentally, in Figure 38, by turning on and off the transistor 11e, N-fold pulse driving illustrated in Figures 13, 15, etc. can be implemented. Figure 39 is an explanatory diagram illustrating an example employing the current-mirror pixel configuration shown in Figure 38. Reset

driving in the current-mirror pixel configuration will be
described below with reference to Figure 39.

As shown in Figure 39(a), the transistors 11c and 11e
are turned off and the transistor 11d is turned on. Then,
the drain (D) terminal and gate (G) terminal of the
current-programming transistor 11b are short-circuited and
a current Ib flows between them as shown in the figure.
Generally, the transistor 11b has been programmed with current
in the previous field (frame) and is capable of passing current
(this is natural because the gate potential is held in the
capacitor 19 for a period of 1F and image is displayed. However,
current does not flow during a completely black display). In
this state, as the transistor 11e is turned off and the
transistor 11d is turned on, the drive current Ib flows through
the gate (G) terminal of the transistor 11a (gate (G) terminal
and the drain (D) terminal are short-circuited).
Consequently, the gate (G) terminal and drain (D) terminal
of the transistor 11a have the same potential, resetting the
transistor 11a (to a state in which no current flows). Since
the driver transistor 11b shares a common gate (G) terminal
with the current-programming transistor 11a, the driver
transistor 11b is also reset.

The reset mode (in which no current flows) of the
transistors 11a and 11b is equivalent to a state in which a
offset voltage is held in voltage offset canceling mode

described with reference to Figure 51 and the like. That is, in the state in Figure 39(a), the offset voltage is held between the terminals of the capacitor 19 (the offset voltage is a starting voltage at which a current starts to flow: when a voltage equal to or larger than the starting voltage is applied, a current flows through the transistor 11). The offset voltage varies with the characteristics of the transistors 11a and 11b. Thus, in Figure 39(a), a state in which the transistors 11a and 11b do not pass current is maintained in the capacitor 19 in each pixel (the transistors 11a and 11b pass a black display current close to zero, i.e., they have been reset to the starting voltage at which a current starts to flow).

In Figure 39(a), as the reset period becomes longer, a larger Ib current tends to flow, reducing the terminal voltage of the capacitor 19, as in the case of Figure 33(a). Thus, the operation time in Figure 39(a) should be fixed. It has been shown experimentally and analytically that preferably the operation time in Figure 39(a) is from 1 H to 10 Hs (ten horizontal scanning periods) both inclusive. More preferably, it should be from 1 H to 5 Hs or from 20 μsec to 2 msec (both inclusive). This also applies to the drive system in Figure 33.

As in the case of Figure 33(a), if the reset mode in Figure 39(a) is synchronized with the current-programming mode in Figure 39(b), there is no problem because the period from the

reset mode in Figure 39(a) to the current-programming mode in Figure 39(b) is fixed (constant). That is, preferably the period from the reset mode in Figure 33(a) or Figure 39(a) to the current-programming mode in Figure 33(b) or Figure 39(b) should be from 1 H to 10 Hs (ten horizontal scanning periods) both inclusive. More preferably, it should be from 1 H to 5 Hs or from 20 μsec to 2 msec (both inclusive). If this period is short, the driver transistors 11 are not reset completely. If it is too long, the driver transistor 11 is turned off completely, which means that much time is required for current programming. Also, the brightness of the screen 50 is decreased.

After the state in Figure 39(a), a state shown in Figure 39(b) occurs. Figure 39(b) shows a state in which the transistors 11c and 11d are turned on and the transistor 11e is turned off. This is a state in which current programming is being performed. Specifically, a programming current Iw is output (absorbed) from the source driver circuit 14 and passed through the current programming transistor 11a. The potential of the gate (G) terminal of the driver transistor 11a is set in the capacitor 19 so that the programming current Iw will flow.

If the programming current Iw is 0 A (black display), the transistor 11b is held in the state in Figure 33(a) in which it does not pass current, and thus proper black display

is achieved. Also, when performing current programming for white display in Figure 39(b), the current programming is started from offset voltage of completely black display even if there are variations in the characteristics of driver transistors in pixels (the offset voltage is a starting voltage at which a current specified according to the characteristics of each driver transistor starts to flow). Thus, the time required to reach a target current value becomes uniform according to gradations. This eliminates gradation errors due to variations in the characteristics of the transistor 11a or 11b, making it possible to achieve proper image display.

After the current programming in Figure 39(b), the transistors 11c and 11d are turned off in sequence and the transistor 11e is turned on to deliver the programming current Iw (= Ie) to the EL element 15 from the driver transistor 11b, and thereby illuminate the EL element 15. What is shown in Figure 39(c) has already been described, and thus detailed description thereof will be omitted.

The drive system (reset driving) described with reference to Figures 33 and 39 consists of a first operation of disconnecting the driver transistor 11a or 11b from the EL element 15 (using the transistor 11e or 11d so that no current flows) and shorting between the drain (D) terminal and gate (G) terminal of the driver transistor (or between the source (S) terminal and gate (G) terminal, or generally speaking,

between two terminals including the gate (G) terminal of the driver transistor) and a second operation of programming the driver transistor with current (voltage) after the first operation.

At least the second operation is performed after the first operation. Incidentally, the operation of disconnecting the driver transistor 11a or 11b from the EL element 15 in the first operation is not absolutely necessary. The drain (D) terminal and gate (G) terminal of the driver transistor are short-circuited in the first operation without disconnecting the driver transistor 11a or 11b from the EL element 15, nothing more than some variations in reset mode may result. Whether to omit disconnection should be determined by considering the characteristics of the transistors in the constructed array.

The current-mirror pixel configuration in Figure 39 provides a drive method which resets the current-programming transistor 11a, and consequently resets the driver transistor 11b.

With the current-mirror pixel configuration in Figure 39, it is not always necessary to disconnect the driver transistor 11b from the EL element 15 in reset mode. Thus, the following operations are performed: a first operation of shorting between the drain (D) terminal and gate (G) terminal of the current-programming transistor a (or between the source (S) terminal and gate (G) terminal, or generally speaking,

between two terminals including the gate (G) terminal of the current-programming transistor or between two terminals including the gate (G) terminal of the driver transistor) and a second operation of programming the current-programming transistor with current (voltage) after the first operation. At least the second operation is performed after the first operation.

In image display mode (if instantaneous changes can be observed), the pixel row to be programmed with current is reset (black display mode) and is programmed with current after a predetermined H. The pixel row of black display moves from top to bottom of the screen and it should look as if the image were rewritten at the location where the pixel row passed by.

Although the above example has been described mainly in relation to pixel configuration for current programming, the reset driving according to the present invention can also be applied to pixel configuration for voltage programming. Figure 43 is an explanatory diagram illustrating a pixel configuration (panel configuration) according to the present invention used to perform reset driving in a pixel configuration for voltage programming.

In the configuration shown in Figure 43, a transistor 11e which resets a driver transistor 11a has been formed. When a turn-on voltage is applied to a gate signal line 17e, the transistor 11e turns on, causing a short circuit between the

gate (G) terminal and drain (D) terminal of the driver
transistor 11a. Also a transistor 11d which cuts off a current
path between the EL element 15 and driver transistor 11a has
been formed. The reset driving according to the present
invention in a pixel configuration for voltage programming
will be described below with reference to Figure 44.

As illustrated in Figure 44(a), the transistors 11b and
11d are turned off and the transistor 11e is turned on. The
drain (D) terminal and gate (G) terminal of the driver
transistor 11a are short-circuited and a current Ib flows as
shown in the figure. Consequently, the gate (G) terminal and
drain (D) terminal of the transistor 11a have the same potential,
resetting the transistor 11a (to a state in which no current
flows). Before resetting the transistor 11a, the transistor
11d is turned on, the transistor 11e is turned off, and current
is passed through the transistor 11a in sync with an HD
synchronization signal as described with reference to Figure
33 or 39. Then the operation shown in Figure 44(a) is
performed.

The reset mode (in which no current flows) of the
transistors 11a and 11b is equivalent to a state in which an
offset voltage is held in voltage offset canceling mode
described with reference to Figure 41 and the like.
That is, in the state in Figure 44(a), the offset voltage (reset
voltage) is held between the terminals of the capacitor 19.

The reset voltage varies with the characteristics of the driver transistor 11a. Thus, in Figure 44(a), a state in which the driver transistors 11a do not pass current is maintained in the capacitor 19 in each pixel (the transistor 11a passes a black display current close to zero, i.e., it has been reset to the starting voltage at which a current starts to flow).

Incidentally, in the pixel configuration for voltage programming, as the reset period becomes longer, a larger Ib current tends to flow, reducing the terminal voltage of the capacitor 19, as in the case of pixel configuration for current programming. Thus, the operation time in Figure 44(a) should be fixed. Preferably, the operation time should be from 0.2 H to 5 Hs (five horizontal scanning periods) both inclusive. More preferably, it should be from 0.5 H to 4 Hs or from 2 μsec to 400 μsec (both inclusive).

Besides, it is preferable that the gate signal line 17e should be shared with the gate signal line 17a in a preceding stage. That is the gate signal line 17e should be shorted to the gate signal line 17a in the pixel row in the preceding stage. This configuration is referred to as a preceding-stage gate control system. Incidentally, the stage-stage gate control system uses waveforms of gate signal lines of a pixel row selected one or more Hs before the pixel row of interest. Thus, this system is not limited to the previous pixel row. For example, the driver transistor 11a of the pixel row of

interest may be reset using the waveforms of gate signal lines
two pixel rows ahead.

The stage-stage gate control system will be described
more concretely. Suppose, the pixel row of interest is the
(N)-th pixel row whose gate signal lines are 17e(N) and 17a(N).
The preceding pixel row selected 1 H before is assumed to be
the (N - 1)-th pixel row whose gate signal lines are 17e(N
- 1) and 17a(N - 1). The pixel row selected 1 H after the
pixel row of interest is assumed to be the (N + 1)-th pixel
row whose gate signal lines are 17e(N + 1) and 17a(N + 1).

In the (N - 1)-th H-period, as a turn-on voltage is applied
to the gate signal line 17a(N - 1) of the (N - 1)-th pixel
row, a turn-on voltage is also applied to the gate signal line
17e(N) of the (N)-th pixel row. This is because the gate signal
line 17e(N) and the gate signal line 17a(N - 1) of the pixel
row in the preceding stage are shorted. Consequently, the
pixel transistor 11b(N - 1) in the (N - 1)-th pixel row is
turned on and the voltage applied to the source signal line
18 is written into the gate (G) terminal of the driver transistor
11a(N - 1). At the same time, the pixel transistor 11e(N)
in the (N)-th pixel row is turned on, the gate (G) terminal
and drain (D) terminal of the driver transistor 11a(N) are
shorted, and the driver transistor 11a(N) is reset.

In the (N)-th H-period which follows the (N - 1)-th
H-period, as a turn-on voltage is applied to the gate signal

line 17a(N) of the (N)-th pixel row, a turn-on voltage is also applied to the gate signal line 17e(N + 1) of the (N + 1)-th pixel row. Consequently, the pixel transistor 11b(N) in the (N)-th pixel row is turned on and the voltage applied to the source signal line 18 is written into the gate (G) terminal of the driver transistor 11a(N). At the same time, the pixel transistor 11e(N + 1) in the (N + 1)-th pixel row is turned on, the gate (G) terminal and drain (D) terminal of the driver transistor 11a(N + 1) are shorted, and the driver transistor 11a(N + 1) is reset.

Similarly, in the (N + 1)-th period which follows the (N)-th H-period, as a turn-on voltage is applied to the gate signal line 17a(N + 1) of the (N + 1)-th pixel row, a turn-on voltage is also applied to the gate signal line 17e(N + 2) of the (N + 2)-th pixel row. Consequently, the pixel transistor 11b(N + 1) in the (N + 1)-th pixel row is turned on and the voltage applied to the source signal line 18 is written into the gate (G) terminal of the driver transistor 11a(N + 1). At the same time, the pixel transistor 11e(N + 2) in the (N + 2)-th pixel row is turned on, the gate (G) terminal and drain (D) terminal of the driver transistor 11a(N + 2) are shorted, and the driver transistor 11a(N + 2) is reset.

According to the above-described stage-stage gate control system of the present invention, the driver transistor

11a is reset for a period of 1 H, and then voltage (current) programming is performed.

As in the case of Figure 33(a), if the reset mode in Figure 44(a) is synchronized with the voltage-programming mode in Figure 44(b), there is no problem because the period from the reset mode in Figure 44(a) to the current-programming mode in Figure 44(b) is fixed (constant). If this period is short, the driver transistors 11 are not reset completely. If it is too long, the driver transistor 11a is turned off completely, which means that much time is required for current programming. Also, the brightness of the screen 12 is decreased.

After the state in Figure 44(a), a state shown in Figure 44(b) occurs. Figure 44(b) shows a state in which the transistor 11b is turned on and the transistors 11e and 11d are turned off. This state in Figure 44(b), is a state in which voltage programming is being performed. Specifically, a programming voltage is output from the source driver circuit 14 and written into the gate (G) terminal of the driver transistor 11a (the potential of the gate (G) terminal of the driver transistor 11a is set in the capacitor 19). Incidentally, in the case of voltage programming, it is not always necessary to turn off the transistor 11d during voltage programming. Besides, the transistor 11e is not necessary if there is no need to combine with the N-fold driving shown in Figure 13, 15, or the like or perform intermittent N/K-fold

pulse driving (this driving method provides two or more illuminated areas in a screen and can be implemented easily by turning on and off the transistor 11e). Since this has been described earlier, description thereof will be omitted.

When performing voltage programming for white display using the configuration shown in Figure 43 or drive method shown in Figure 44, the voltage programming is started from offset voltage of completely black display even if there are variations in the characteristics of driver transistors in pixels (the offset voltage is a starting voltage at which a current specified according to the characteristics of each driver transistor starts to flow). Thus, the time required to reach a target current value becomes uniform according to gradations. This eliminates gradation errors due to variations in the characteristics of the transistor 11a, making it possible to achieve proper image display.

After the current programming in Figure 44(b), the transistor 11d is turned off and the transistor 11d is turned on to deliver the programming current to the EL element 15 from the driver transistor 11a, and thereby illuminate the EL element 15, as shown in Figure 44(c).

As described above, the reset driving according to the present invention using the voltage programming shown in Figure 43 consists of a first operation of turning on the transistor 11d, turning off the transistor 11e, and passing current

through the transistor 11a in sync with the HD synchronization signal; a second operation of disconnecting the transistor 11a from the EL element 15 and shorting between the drain (D) terminal and gate (G) terminal of the driver transistor 11a (or between the source (S) terminal and gate (G) terminal, or generally speaking, between two terminals including the gate (G) terminal of the driver transistor); and a third operation of programming the driver transistor 11a with voltage after the above operations.

In the above example, the transistor 11d is turned on and off to control the current delivered from the driver transistor element 11a (in the case of configuration shown in Figure 1) to the EL element 15. To turn on and off the transistor 11d, the gate signal line 17b needs to be scanned, for which the shift register circuit 61 (the gate driver circuit 12) is required. However, shift register circuits 61 are large in scale and the use of a shift register circuit 61 for the gate signal line 17b makes it impossible to reduce bezel width. A system described with reference to Figure 40 solves this problem.

Incidentally, although the pixel configuration for current programming illustrated in Figure 1 and the like is mainly described herein by way of examples, the present invention is not limited to this and it goes without saying that the present invention can also be applied to other

configuration for current programming (current-mirror pixel configuration) described with reference to Figure 38 and the like. Also, the technical concept of turning on and off elements as a block can also be applied to the pixel configuration for voltage programming in Figure 41 and the like.

According to the invention, since this method passes current through the EL elements 15 intermittently, it can be used in combination with a method (described with reference to Figure 50, etc.) which applies a reverse bias voltage.

Thus, reset driving can be performed in combination with other examples according to the present invention.

Figure 40 shows an example of a block driving system. For ease of understanding, it is assumed that a gate driver circuit 12 is formed directly on a board 71 or that a silicon chip, gate driver IC 12, is mounted on a board 71. Source driver circuits 14 and source signal lines 18 are omitted to avoid complicating the drawing.

In Figure 40, gate signal lines 17a are connected to the gate driver circuit 12. On the other hand, gate signal lines 17b are connected to illumination control lines 401. In Figure 40, four gate signal lines 17b are connected to one illumination control line 401.

Incidentally, although four gate signal lines 17b are grouped into a block here, this is not restrictive and it goes

without saying that more than four gate signal lines 17b may be grouped into a block. Generally, it is preferable to divide the screen 50 into five or more parts. More preferably, the screen 50 should be divided into ten or more parts. Even more preferably, the screen 50 should be divided into twenty or more parts. A small number of divisions will make flickering conspicuous. Too large a number of divisions will increase the number of illumination control lines 401, making it difficult to lay out the illumination control lines 401.

Thus, in the case of a QCIF display panel, which has 220 vertical scanning lines, at least 220/5 = 44 or more lines should be grouped into a block. More preferably, 220/10 = 11 or more lines should be grouped into a block. However, if odd-numbered rows and even-numbered rows are grouped into two different blocks, there is not much flickering even at a low frame rate, and thus the two blocks are sufficient.

In the example shown in Figure 40, the current flowing through the EL elements 15 are turned on and off on a block-by-block basis by the application of either a turn-on voltage (Vgl) or turn-off voltage (Vgh) to illumination control lines 401a, 401b, 401c, 401d, ..., 401n in sequence.

Incidentally, in the example in Figure 40, the gate signal lines 17b do not intersect the illumination control lines 401. Thus, there can be no defect in which a gate signal line 17b would become short-circuited with an illumination control line

401. Also, since there is no capacitive coupling between gate signal lines 17b and illumination control lines 401, addition of capacitance is very small when the gate signal lines 17b are viewed from the illumination control lines 401. This makes it easy to drive the illumination control lines 401.

The gate driver circuit 12 is connected with the gate signal lines 17a. When a turn-on voltage is applied to gate signal lines 17a, the appropriate pixel rows are selected and the transistors 11b and 11c in the selected pixel rows are turned on. Then, currents (voltage) applied to the source signal lines 18 are programmed into the capacitors 19 in the pixels. On the other hand, the gate signal lines 17b are connected with the gate (G) terminals of the transistors 11d in the pixels. Thus, when a turn-on voltage (Vgl) is applied to the illumination control lines 401, current paths are formed between the driver transistors 11a and EL elements 15. When a turn-off voltage (Vgh) is applied, the anode terminals of the EL elements 15 are opened.

Preferably, control timing of turn-on/turn-off voltages applied to the illumination control lines 401 and a pixel row selection voltage (Vgl) outputted to the gate signal lines 17a by the gate driver circuit 12 are synchronized with one horizontal scanning clock (1H). However, this is not restrictive.

The signals applied to the illumination control lines
401 simply turn on and off the current delivered to the EL
elements 15. They do not need to be synchronized with image
data outputted from the source driver circuits 14. This is
because the signals applied to the illumination control lines
401 are intended to control the current programmed into the
capacitors 19 in the pixels 16. Thus, they do not always need
to be synchronized with the pixel row selection signal. Even
when they are synchronized, the clock is not limited to a 1-H
signal and may be a 1/2-H or 1/4-H signal.

Even in the case of the current-mirror pixel configuration
shown in Figure 38, the transistors 11e can be turned on and
off if the gate signal lines 17b are connected to the
illumination control lines 401. Thus, block driving can be
implemented.

Incidentally, in Figure 32, by connecting the gate signal
lines 17a to the illumination control lines 401 and performing
resets, it is possible to implement block driving. In other
words, the block driving according to the present invention
is a drive method which puts a plurality of pixel rows in
non-illumination (black display) mode simultaneously using
one control line.

In the above example, one selection pixel row is placed
(formed) per pixel row. The present invention is not limited

to this and a selection gate signal line may be placed (formed) for two or more pixel rows.

Figure 41 shows such an example. Incidentally, for ease of explanation, the pixel configuration in Figure 1 is employed mainly. In Figure 41, the gate signal line 17a for pixel row selection selects three pixels (16R, 16G, and 16B) simultaneously. Reference character R is intended to indicate something related to a red pixel, reference character G indicates something related to a green pixel, and reference character B indicates something related to a blue pixel.

Thus, when the gate signal line 17a is selected, the pixels 16R, 16G, and 16B are selected and get ready to write data. The pixel 16R writes data into a capacitor 19R via a source signal line 18R, the pixel 16G writes data into a capacitor 19G via a source signal line 18G, and the pixel 16B writes data into a capacitor 19B via a source signal line 18B.

The transistor 11d of the pixel 16R is connected to a gate signal line 17bR, the transistor 11d of the pixel 16G is connected to a gate signal line 17bG, and the transistor 11d of the pixel 16B is connected to a gate signal line 17bB. Thus, an EL element 15R of the pixel 16R, EL element 15G of the pixel 16G, and EL element 15B of the pixel 16B can be turned on and off separately. Illumination times and illumination periods of the EL element 15R, EL element 15G, and EL element

15B can be controlled separately by controlling the gate signal line 17bR, gate signal line 17bG, and gate signal line 17bB.

To implement this operation, in the configuration in Figure 6, it is appropriate to form (place) four shift register circuits: a shift register circuit 61 which scans the gate signal line 17a, shift register circuit 61 which scans the gate signal line 17bR, shift register circuit 61 which scans the gate signal line 17bG, and shift register circuit 61 which scans the gate signal line 17bB.

Incidentally, although it has been stated that a current N times larger than a predetermined current is passed through the source signal line 18 and that a current N times larger than a predetermined current is passed through the EL element 15 for a period of 1/N, this cannot be implemented in practice. Actually, signal pulses applied to the gate signal line 17 penetrate into the capacitor 19, making it impossible to set a desired voltage value (current value) on the capacitor 19. Generally, a voltage value (current value) lower than a desired voltage value (current value) is set on the capacitor 19. For example, even if 10 times larger current value is meant to be set, only approximately 5 times larger current value is set on the capacitor 19. For example, even if N = 10 is specified, N = 5 times larger current actually flows through the EL element 15. Thus, this method sets an N times larger current value to pass a current proportional or corresponding to the N-fold

value through the EL element 15. Alternatively, this drive method applies a current larger than a desired value to the EL element 15 in a pulsed manner.

This method performs current (voltage) programming so as to obtain desired emission brightness of the EL element by passing a current larger than a desired value intermittently through the driver transistor 11a (in the case of Figure 1) (i.e., a current which will give brightness higher than the desired brightness if passed through the EL element 15 continuously).

Incidentally, a compensation circuit which employs the penetration to the capacitor 19 is installed in the source driver circuit 14. This will be described later.

Preferably, N-channel transistors are used as the switching transistors 11b and 11c, etc. in Figure 1 and the like. This will reduce penetration voltage reaching the capacitor 19. Also, since off-leakage of the capacitor 19 is reduced, this method can be applied to a 10-Hz or lower frame rate.

Depending on pixel configuration, if the penetration voltage tends to increase the current flowing through the EL element 15, white peak voltage will increase, increasing perceived contrast in image display. This provides for a good image display.

Conversely, it is also useful to use P-channel transistors as the switching transistors 11b and 11c in Figure 1 to cause penetration, and thereby obtain a proper black display. When the P-channel transistor 11b turns off, the voltage goes high (Vgh), shifting the terminal voltage of the capacitor 19 slightly to the Vdd side. Consequently, the voltage at the gate (G) terminal of the transistor 11a rises, resulting in more intense black display. Also, the current used for first gradation display can be increased (a certain base current can be delivered up until gradation 1), and thus shortages of write current can be eased during current programming.

Another drive method according to the present invention will be described below with reference to drawings. Figure 174 is an explanatory diagram illustrating a display panel which performs sequential driving according to the present invention. A source driver circuit 14 outputs R, G, and B data to connection terminals 761 by switching among them. Thus, the source driver circuit 14 only needs 1/3 as many output terminals as in Figure 48.

Signals outputted from the source driver circuit 14 to the connection terminals 761 are allocated to 18R, 18G, and 18B by an output switching circuit 1741. The output switching circuit 1741 is formed directly on a board 71 by polysilicon technology. Alternatively, the output switching circuit 1741 may be formed with silicon chips and mounted on the board 71

by COG technology. Also, the output switching circuit 1741 may be incorporated into the source driver circuit 14 as a sub-circuit of the source driver circuit 14.

If a changeover switch 1742 is connected to an R terminal, the output signal from the source driver circuit 14 is applied to the source signal line 18R. If the changeover switch 1742 is connected to a G terminal, the output signal from the source driver circuit 14 is applied to the source signal line 18G. If the changeover switch 1742 is connected to a B terminal, the output signal from the source driver circuit 14 is applied to the source signal line 18B.

Incidentally, in the configuration in Figure 175, when the changeover switch 1742 is connected to the R terminal, the G terminal and B terminal of the changeover switch are open. Thus, the current entering the source signal lines 18G and 18B is 0 A. Consequently, the pixels 16 connected to the source signal lines 18G and 18B provide a black display.

When the changeover switch 1742 is connected to the G terminal, the R terminal and B terminal of the changeover switch are open. Thus, the current entering the source signal lines 18R and 18B is 0 A. Consequently, the pixels 16 connected to the source signal lines 18R and 18B provide a black display.

In the configuration in Figure 175, when the changeover switch 1742 is connected to the B terminal, the R terminal and G terminal of the changeover switch are open. Thus, the

current entering the source signal lines 18R and 18G is 0 A.
Consequently, the pixels 16 connected to the source signal
lines 18R and 18G provide a black display.

Basically, if one frame consists of three fields, R image
data is written in sequence into the pixels 16 in the screen
50 in the first field. In the second field, G image data is
written in sequence into the pixels 16 in the screen 50. In
the third field, B image data is written in sequence into the
pixels 16 in the screen 50.

Thus, R data → G data → B data → R data → ... are rewritten
in sequence in the appropriate fields to implement sequential
driving. Description of how N-fold pulse driving is performed
by turning on and off the switching transistor 11d as shown
in Figure 1 has been given with reference to Figures 5, 13,
16, etc. Needless to say, such a drive method can be combined
with sequential driving. Of course, it goes without saying
that other drive methods according to the present invention
can be combined with sequential driving.

In the above example, it has been stated that when image
data is written into the R pixel 16, black data is written
into the G pixel and B pixel, that when image data is written
into the G pixel 16, black data is written into the R pixel
and B pixel, and that when image data is written into the B
pixel 16, black data is written into the R pixel and G pixel.
The present invention is not limited to this.

For example, when image data is written into the R pixel 16, the G pixel and B pixel may retain the image data rewritten in the previous field. This can make the screen 50 brighter. When image data is written into the G pixel 16, the R pixel and B pixel may retain the image data rewritten in the previous field. When image data is written into the B pixel 16, the G pixel and R pixel may retain the image data rewritten in the previous field.

In order to retain image data in pixels other than the color pixel being rewritten, the gate signal line 17a can be controlled separately for the R, G, and B pixels. For example, as illustrated in Figure 174, a gate signal line 17aR can be designated as a signal line which turns on and off the transistors 11b and 11c of the R pixel, a gate signal line 17aG can be designated as a signal line which turns on and off the transistors 11b and 11c of the G pixel, and a gate signal line 17aB can be designated as a signal line which turns on and off the transistors 11b and 11c of the B pixel. On the other hand, the gate signal line 17b can be designated as a signal line which commonly turns on and off the transistors 11d of the R, G, and B pixels.

With the above configuration, when the source driver circuit 14 outputs R image data and the changeover switch 1742 is set to an R contact, a turn-on voltage can be applied to the gate signal line 17aR and a turn-off voltage can be applied

to the gate signal lines aG and aB. Thus, the R image data
can be written into the R pixel 16 and the G pixel 16 and R
pixel 16 can retain the image data of the previous field.

When the source driver circuit 14 outputs G image data
in the second field and the changeover switch 1742 is set to
a G contact, a turn-on voltage can be applied to the gate signal
line 17aG and a turn-off voltage can be applied to the gate
signal lines aR and aB. Thus, the G image data can be written
into the G pixel 16 and the R pixel 16 and B pixel 16 can retain
the image data of the previous field.

When the source driver circuit 14 outputs B image data
in the third field and the changeover switch 1742 is set to
a B contact, a turn-on voltage can be applied to the gate signal
line 17aB and a turn-off voltage can be applied to the gate
signal line aR and aG. Thus, the B image data can be written
into the B pixel 16 and the R pixel 16 and G pixel 16 can retain
the image data of the previous field.

In the example shown in Figure 174, the gate signal lines
17a are placed (formed) in such a way as to turns on and off
the transistors 11b of the R, G, and B pixels 16 separately.
However, the present invention is not limited to this. For
example, a gate signal line 17a common to the R, G, and B pixels
16 may be formed of placed as illustrated in Figure 175.

In relation to the configuration in Figure 174 and the
like, it has been stated that when the R source signal line

is selected by the changeover switch 1742, the G and B source signal lines are open. However, the open state is an electrically floating state and is not desirable.

Figure 175 shows a configuration in which measures are taken to eliminate such floating state. A terminal a of a changeover switch 1742 of an output switching circuit 1741 is connected to a Vaa voltage (voltage for black display). A terminal b is connected to an output terminal of the source driver circuit 14. The changeover switch 1742 is installed for each of the R, G, and B pixels.

In the state shown in Figure 175, a changeover switch 1742R is connected to a Vaa terminal. Thus, the Vaa voltage (voltage for black display) is applied to the source signal line 18R. A changeover switch 1742G is connected to a Vaa terminal. Thus, the Vaa voltage (voltage for black display) is applied to the source signal line 18G. A changeover switch 1742B is connected to the output terminal of the source driver circuit 14. Thus, a B image signal is applied to the source signal line 18B.

In the above state, the B pixel is being rewritten and a black display voltage is applied to the R pixel and G pixel. As the changeover switches 1742 are controlled in the above manner, an image composed of the pixels 16 are rewritten. Incidentally, control of the gate signal lines 17b is the same

as in the examples described above, and thus detailed description thereof will be omitted.

In the above example, the R pixel 16 is rewritten in the first field, the G pixel 16 is rewritten in the second field, and the B pixel 16 is rewritten in the third field. That is, the color of the pixel rewritten changes every field. The present invention is not limited to this. The color of the pixel rewritten may be changed every horizontal scanning period (1 H). For example, a possible drive method involves rewriting the R pixel in the first H, the G pixel in the second H, the B pixel in the third H, the R pixel in the fourth H, and so on. Of course, the color of the pixel rewritten may be changed every two horizontal scanning periods or every 1/3 field.

Figure 176 shows an example, in which the color of the pixel rewritten changes every 1 H. Incidentally, in Figures 176 to 178, the oblique hatching indicates that the pixels 16 either retain image data from the previous field instead of being rewritten or are displayed in black. Of course, the black display of the pixels and retention of image data from the previous field may be repeated alternately.

Needless to say, in the drive system in Figures 174 to 178, it is also possible to use the N-fold pulse driving in Figure 13 or simultaneous M-row driving. Figures 174 to 178 show writing of pixels 16. Although illumination control of the EL elements 15 is not described, it goes without saying

that this example can be used in combination with examples described earlier or later.

One frame need not necessarily consist of three fields and may consist of two fields or four or more fields. In one example illustrated herein, one frame consists of two fields and the R and G pixels out of the three primary RGB colors are rewritten in the first field and the B pixel is rewritten in the second field. In another example illustrated herein, one frame consists of four fields and the R pixel out of the three primary RGB colors is rewritten in the first field, the G pixel is rewritten in the second field, and the B pixel is rewritten in the third and fourth field. In these sequences, white balance can be achieved more efficiently if the luminous efficiencies of the R, G, and B EL elements 15 are taken into consideration.

In the above example, the R pixel 16 is rewritten in the first field, the G pixel 16 is rewritten in the second field, and the B pixel 16 is rewritten in the third field. That is, the color of the pixel rewritten changes every field.

According to the example shown in Figure 176, in the first field, an R pixel is rewritten in the first H, a G pixel is rewritten in the second H, a B pixel is rewritten in the third H, an R pixel is rewritten in the fourth H, and so on. Of course, the color of the pixel rewritten may be changed every two or more horizontal scanning periods or every 1/3 field.

According to the example shown in Figure 176, in the first field, an R pixel is rewritten in the first H, a G pixel is rewritten in the second H, a B pixel is rewritten in the third H, and an R pixel is rewritten in the fourth H. In the second field, a G pixel is rewritten in the first H, a B pixel is rewritten in the second H, an R pixel is rewritten in the third H, and a G pixel is rewritten in the fourth H. In the third field, a B pixel is rewritten in the first H, an R pixel is rewritten in the second H, a G pixel is rewritten in the third H, and a B pixel is rewritten in the fourth H.

Thus, by rewriting the R, G, and B pixels in each field arbitrarily or with some regularity, it is possible to prevent separation among the R, G, and B colors. Also, flickering is reduced.

In Figure 177, a plurality of pixel 16 colors are rewritten every 1 H. In Figure 176, in the first field, the pixel 16 rewritten in the first H is an R pixel, the pixel 16 rewritten in the second H is a G pixel, the pixel 16 rewritten in the third H is a B pixel, the pixel 16 rewritten in the fourth H is an R pixel.

In Figure 177, positions of the different-colored pixels rewritten are changed every 1 H. By assigning R, G, and B pixels to different fields (needless to say, this may be done with some regularity) and rewriting them in sequence, it is

possible to prevent separation among the R, G, and B colors as well as to reduce flickering.

Incidentally, even in the example in Figure 177, the R, G, and B pixels should have the same illumination time or luminous intensity in each picture element, which is a set of R, G, and B pixels. Needless to say, this is also done in the examples in Figures 175, 176, and the like to avoid color irregularities.

As shown in Figure 177, in order to rewrite pixels of different colors in each H (three colors--R, G, and B--are rewritten in the first H in the first field in Figure 177), in Figure 174, the source driver circuit 14 can be configured to output image signals of arbitrary colors (or colors determined with some regularity) to the terminals and the changeover switches 1742 can be configured to connect to the R, G, and B contacts arbitrarily (or with some regularity).

The panel in an example in Figure 178 has W (white) pixels 16W in addition to the three primary colors RGB. By forming or placing pixels 16W, it is possible to achieve peak brightness of colors properly as well as to achieve a high brightness-display. Figure 178(a) shows an example in which R, G, B, and W pixels 16 are formed in each pixel row. Figure 178(b) shows an example in which R, G, B, and W pixels are placed in turns in different pixel rows.

Needless to say, the drive method in Figure 178 can incorporate the drive methods in Figures 176, 177, etc. Also, it goes without saying that N-fold pulse driving, simultaneous M-row driving, etc. can be incorporated. These matters can easily be implemented by those skilled in the art based on this specification, and thus description thereof will be omitted.

Incidentally, for ease of explanation, it is assumed that the display panel according to the present invention has the three primary colors RGB, but this is not restrictive. The display panel may have cyan, yellow, and magenta in addition to R, G, and B, or it may have any one of R, G, and B or any two of R, G, and B.

Also, although it has been stated that the sequential driving system handles R, G, and B in each field, it goes without saying that the present invention is not limited to this. Besides, the examples in Figures 174 to 178 illustrate how image data is written into pixels 16. They do not illustrate (although, of course, they are related to) a method of displaying images by operating the transistors 11d and passing current through the EL elements 15 unlike in Figure 1. In the configuration shown in Figure 1, current is passed through the EL elements 15 by controlling the transistors 11d.

Also, the drive methods in Figures 176, 177, etc. can display RGB images in sequence by controlling the transistors

11d (in the case of Figure 1). For example, in Figure 179(a), an R display area 53R, G display area 53G, and B display area 53B are scanned from top to bottom (or from bottom to top) of the screen during one frame (one field) period. The remaining area becomes a non-display area 52. That is, intermittent driving is performed.

Figure 179(b) shows an example in which a plurality of RGB display areas 53 are generated during one field (one frame) period. This drive method is analogous to the one shown in Figure 16. Thus, it will require no explanation. In Figure 179(b), by dividing the display area 53, it is possible to eliminate flickering even at a lower frame rate.

Figure 180(a) shows a case in which R, G, and B display areas 53 have different sizes (needless to say, the size of a display area 53 is proportional to its illumination period). In Figure 180(a), the R display area 53R and G display area 53G have the same size. The B display area 53B has a larger size than the G display area 53G.
With organic EL display panels, B often has a low luminous efficiency. By making the B display area 53B larger than the display areas 53 of other colors as shown in Figure 180(a), it is possible to achieve a white balance efficiently.

Figure 180(b) shows an example in which there are a plurality of B display periods 53B (53B1 and 53B2) during one field (one frame) period. Whereas Figure 180(a) shows a method

of varying the size of one B display area 53B to allow the white balance to be adjusted properly, Figure 180(b) shows a method of displaying multiple B display areas 53B having the same surface area to achieve a proper white balance.

The drive system according to the present invention is not limited to either Figure 180(a) or Figure 180(b). It is intended to generate R, G, and B display areas 53 and create an intermittent display, and thereby correct blurred moving pictures and insufficient writing into the pixels 16. With the drive method in Figure 16, independent display areas 53 for R, G, and B are not generated. R, G, and B are displayed simultaneously (it should be stated that a W display area 53 is presented). Incidentally, it goes without saying that Figure 180(a) and Figure 180(b) may be combined. For example, it is possible to combine the drive method of using display areas 53 of different sizes for R, G, and B in Figure 180(a) with the drive method of generating multiple display areas 53 for R, G, or B in Figure 180(b).

Incidentally, the drive method in Figures 179 and 180 is not limited to the drive methods in Figures 174 to 178 according to the present invention. Needless to say, with a configuration in which the currents flowing through the EL elements 15 (EL elements 15R, EL elements 15G, and EL elements 15B) are controlled separately for R, G, and B as shown in Figure 41, the drive method in Figures 179 and 180 can be

implemented easily. By applying turn-on/turn-off voltages to the gate signal line 17bR, it is possible to turn on and off the R pixel 16R. By applying turn-on/turn-off voltages to the gate signal line 17bG, it is possible to turn on and off the G pixel 16G. By applying turn-on/turn-off voltages to the gate signal line 17bB, it is possible to turn on and off the B pixel 16B.

The above driving can be implemented by forming or placing a gate driver circuit 12bR which controls the gate signal line 17bR, a gate driver circuit 12bG which controls the gate signal line 17bG, and a gate driver circuit 12bB which controls the gate signal line 17bB, as illustrated in Figure 181. By driving the gate drivers 12bR, 12bG, and 12bB in Figure 181 by the method described in Figure 6 or the like, the drive method in Figures 179 and 180 can be implemented. Of course, it goes without saying that the drive methods in Figure 16 and the like can be implemented using the configuration of the display panel in Figure 181.

Also, with the configuration shown in Figures 174 to 177, the drive method in Figures 179 and 180 can be implemented using a gate signal line 17b common to the R, G, and B pixels without using a gate signal line 17bR which controls the EL elements 15R, a gate signal line 17bG which controls the EL elements 15G, and a gate signal line 17bB which controls the EL elements 15B as long as black image data can be written

into pixels 16 other than the pixels 16 whose image data is rewritten.

It has been stated with reference to Figures 15, 18, 21, etc. that the gate signal line 17b (EL-side selection signal line) applies a turn-on voltage (Vgl) and turn-off voltage (Vgh) every horizontal scanning period (1 H). However, in the case of a constant current, light emission quantity of the EL elements 15 is proportional to the duration of the current. Thus the duration is not limited to 1 H.

Figure 194 shows 1/4-duty ratio driving. A turn-on voltage is applied to the gate signal line 17b (EL-side selection signal line) for 1 H every 4 Hs and the locations to which the turn-on voltage is applied are scanned in sync with a horizontal synchronization signal (HD). Thus, the unit length of a conduction period is 1 H.

However, the present invention is not limited to this. The duration of the conduction period may be less than 1 H (1/2 H in Figure 197) as shown in Figure 197 or it may be equal to or less than 1 H. In short, the unit length of the conduction period is not limited to 1 H and a unit length other than 1 H can be generated easily. The OEV2 circuit formed or placed in the output stage of the gate driver circuit 12b (circuit which controls the gate signal line 17b) can be used for that.

To introduce a concept of output enable (OEV), the following provisions are made. By performing OEV control, turn-on and turn-off voltages (Vgl voltage and Vgh voltage) can be applied to the pixels 16 from the gate signal line 17a and 17b within one horizontal scanning period (1 H).

For ease of explanation, it is assumed that in the display panel according to the present invention, the pixel rows to be programmed with current are selected by the gate signal line 17a (in the case of Figure 1). The output from the gate driver circuit 12a which controls the gate signal line 17a is referred to as a WR-side selection signal line. Also, it is assumed that EL elements 15 are selected by the gate signal line 17b (in the case of Figure 1). The output from the gate driver circuit 12b which controls the gate signal line 17b is referred to as an EL-side selection signal line.

The gate driver circuits 12 are fed a start pulse, which is shifted as holding data in sequence within a shift register. Based on the holding data in the shift register of the gate driver circuit 12a, it is determined whether to output a turn-on voltage (Vgl) or turn-off voltage (Vgh) to the WR-side selection signal line. An OEV1 circuit (not shown) which turns off output forcibly is formed or placed in an output stage of the gate driver circuit 12a. When the OEV1 circuit is low, a WR-side selection signal which is an output of the gate driver circuit 12a is output as it is to the gate signal line 17a.

The above relationship is illustrated logically in Figure 224(a) (OR circuit). Incidentally, the turn-on voltage is set at logic level L (0) and the turn-off voltage is set at logic voltage H (1).

That is, when the gate driver circuit 12a outputs a turn-off voltage, the turn-off voltage is applied to the gate signal line 17a. When the gate driver circuit 12a outputs a turn-on voltage (logic low), it is ORed with the output of the OEV1 circuit by the OR circuit and the result is output to the gate signal line 17a. That is, when the OEV1 circuit is high, the turn-off voltage (Vgh) is output to the gate driver signal line 17a (see an exemplary timing chart in Figure 224).

Based on holding data in a shift register of the gate driver circuit 12b, it is determined whether to output a turn-on voltage (Vgl) or turn-off voltage (Vgh) to the gate signal line 17b (EL-side selection signal line). An OEV2 circuit (not shown) which turns off output forcibly is formed or placed in an output stage of the gate driver circuit 12b. When the OEV2 circuit is low, an output of the gate driver circuit 12b is output as it is to the gate signal line 17b. The above relationship is illustrated logically in Figure 116(a). Incidentally, the turn-on voltage is set at logic level L (0) and the turn-off voltage is set at logic voltage H (1).

That is, when the gate driver circuit 12b outputs a turn-off voltage (an EL-side selection signal is a turn-off

voltage), the turn-off voltage is applied to the gate signal line 17b. When the gate driver circuit 12b outputs a turn-on voltage (logic low), it is ORed with the output of the OEV2 circuit by the OR circuit and the result is output to the gate signal line 17b. That is, when an input signal is high, the OEV2 circuit outputs the turn-off voltage (Vgh) to the gate driver signal line 17b. Thus, even if the EL-side selection signal from the OEV2 circuit is a turn-on voltage, the turn-off voltage (Vgh) is output forcibly to the gate signal line 17b. Incidentally, if an input to the OEV2 circuit is low, the EL-side selection signal is output directly to the gate signal line 17b (see the exemplary timing chart in Figure 176).

Incidentally, screen brightness is adjusted under the control of OEV2. There are permissible limits to changes in screen brightness. Figure 223 illustrates relationship between permissible changes (%) and screen brightness (nt). As can be seen from Figure 223, relatively dark images have small permissible changes. Thus, in performing brightness adjustments of the screen 50 under the control of OEV2 or through duty cycle control, the brightness of the screen 50 should be taken into consideration. Permissible changes should be shorter when the screen is dark than when it is bright.

In Figure 195, the conduction period of the gate signal line 17b (EL-side selection signal line) does not have a unit length of 1 H. A turn-on voltage little shorter than 1 H is

applied to the gate signal lines 17b (EL-side selection signal lines) in odd-numbered pixel rows. A turn-on voltage is applied to the gate signal lines 17b (EL-side selection signal lines) in even-numbered pixel rows for a very short period. The duration T1 of the turn-on voltage applied to the gate signal lines 17b (EL-side selection signal lines) in odd-numbered pixel rows plus the duration T2 of the turn-on voltage applied to the gate signal lines 17b (EL-side selection signal lines) in even-numbered pixel rows is designed to be 1 H. Figure 195 shows a state of the first field.

In the second field which follows the first field, a turn-on voltage little shorter than 1 H is applied to the gate signal lines 17b (EL-side selection signal lines) in even-numbered pixel rows. A turn-on voltage is applied to the gate signal lines 17b (EL-side selection signal lines) in odd-numbered pixel rows for a very short period. The duration T1 of the turn-on voltage applied to the gate signal lines 17b (EL-side selection signal lines) in even-numbered pixel rows plus the duration T2 of the turn-on voltage applied to the gate signal lines 17b (EL-side selection signal lines) in odd-numbered pixel rows is designed to be 1 H.

The sum duration of turn-on voltage applications to gate signal lines 17b in a plurality of pixel rows may be designed to be constant. Alternatively, the illumination time of each

EL element 15 in each pixel row in each field may be designed to be constant.

Figure 196 shows a case in which the conduction period of the gate signal line 17b (EL-side selection signal line) is 1.5 Hs. The rise and fall of the gate signal line 17b at point A are designed to overlap. The gate signal line 17b (EL-side selection signal line) and source signal line 18 are coupled. Thus, any change in a waveform of the gate signal line 17b (EL-side selection signal line) penetrates to the source signal line 18. Consequently, any potential fluctuation in the source signal line 18 lowers accuracy of current (voltage) programming, causing irregularities in the characteristics of the driver transistors 11a to appear in the display.

Referring to Figure 196, at point A, the voltage applied to the gate signal line 17B (EL-side selection signal line) (1) changes from turn-on voltage (Vgl) to turn-off voltage (Vgh). The voltage applied to the gate signal line 17B (EL-side selection signal line) (2) changes from turn-off voltage (Vgh) to turn-on voltage (Vgl). Thus, at point A, the signal waveform of the gate signal line 17B (EL-side selection signal line) (1) and the signal waveform of the gate signal line 17B (EL-side selection signal line) (2) cancel out each other. Consequently, even if the gate signal line 17B (EL-side selection signal line) and source signal line 18 are coupled,

changes in the waveform of the gate signal line 17b (EL-side selection signal line) do not penetrate to the source signal line 18. This improves the accuracy of current (voltage) programming, resulting in a uniform image display.

Incidentally, in the example in Figure 196, the conduction period is 1.5 Hs. However, the present invention is not limited to this. Needless to say, the duration of application of the turn-on voltage may be 1 H or less as illustrated in Figure 198.

By adjusting the duration of application of the turn-on voltage to the gate signal line 17B (EL-side selection signal line), it is possible to adjust the brightness of the display screen 50 linearly. This can be done easily through control of the OEV2 circuit. Referring to Figure 199, for example, display brightness in Figure 199(b) is lower than in Figure 199(a). Also, display brightness in Figure 199(c) is lower than in Figure 199(b).

As shown in Figure 200, multiple sets of turn-on voltage and turn-off voltage may be applied in a period of 1 H. Figure 200(a) shows an example in which six sets are applied. Figure 200(b) shows an example in which three sets are applied. Figure 200(c) shows an example in which one set is applied. In Figure 200, display brightness is lower in Figure 200(b) than in Figure 200(a). It is lower in Figure 200(c) than in Figure 200(b).

Thus, by controlling the number of conduction periods, display brightness can be adjusted (controlled) easily.

One of the problems with the N-fold pulse driving according to the present invention is that a current N times larger than in the case of the conventional is applied to the EL element 15 although instantaneously. A large current may lower the life of the EL element. To solve this problem, it may be useful to apply a reverse bias voltage Vm to the EL element.

Application of a reverse bias voltage means application of a reverse current, and thus injected electrons and positive holes are drawn to the negative and positive poles, respectively. This makes it possible to cancel formation of space charge in the organic layer and reduce electro-chemical degradation, thereby prolonging the life.

Figure 45 shows reverse bias voltage Vm versus changes in terminal voltage of the EL element 15. The terminal voltage results when a rated current is applied to the EL element 15. In Figure 45, the current density of the current passed through the EL element 15 is 100 A per square meter. The trend in Figure 45 shows little difference from the trend observed when the current density is 50 to 100 A per square meter. Thus, it is presumed that this method can be applied to a wide range of current density.

The vertical axis represents the ratio of the terminal voltage after 2500 hours to the initial terminal voltage of

the EL element 15.

For example, if the terminal voltage is 8 V and 10 V, respectively, when a current with a current density of 100 A per square meter is applied at time 0 (zero) and after 2500 hours, the terminal voltage ratio is 10/8 = 1.25.

The horizontal axis represents the ratio of the product of the reverse bias voltage Vm and its application duration t1 in a period to a rated terminal voltage V0. For example, if the reverse bias voltage Vm is applied at 60 Hz (60 Hz has no particular meaning) for 1/2 (half) a period, then t1 = 0.5. Also, if the terminal voltage (rated terminal voltage) is 8 V when a current with a current density of 100 A per square meter is applied at time 0 (zero) and if the reverse bias voltage Vm is 8 V, then |reverse bias voltage × t1|/(rated terminal voltage × t2) = |-8 (V) × 0.5|/(8 (V) × 0.5) = 1.0.

In Figure 45, the terminal voltage ratio stops to change when |reverse bias voltage × t1|/(rated terminal voltage × t2) is 1.0 or larger (no change to the initial rated terminal voltage). Consequently, the application of the reverse bias voltage Vm works well. However, the terminal voltage ratio tends to increase when |reverse bias voltage × t1|/(rated terminal voltage × t2) is 1.75 or larger. Thus, the reverse bias voltage Vm and the application duration rate t1 (or t2 or the ratio between t1 and t2) should be determined in such a way as to make |reverse bias voltage × t1|/(rated terminal

voltage × t2) equal to or larger than 1.0. Preferably, the reverse bias voltage Vm and the application duration rate t1 should be determined in such a way as to make |reverse bias voltage × t1| / (rated terminal voltage × t2) equal to or smaller than 1.75.

However, for bias driving, the reverse bias Vm and rated current should be applied alternately. To equalize average brightness of samples A and B over a unit time as shown in Figure 46 by the application of the reverse bias voltage Vm, it is necessary to pass a larger current instantaneously than when no reverse bias voltage is applied. Consequently, the application of the reverse bias voltage Vm (sample A in Figure 46) also increases the terminal voltage of the EL element 15.

However, in Figure 45, even with the drive method which involves applying the reverse bias voltage, the rated terminal voltage V0 should satisfy the average brightness (i.e., illuminate the EL element 15). (According to examples cited herein, such a terminal voltage is obtained when a current with a current density of 200 A per square meter is applied. However, since the duty ratio is 1/2 the average brightness over one cycle is equal to the brightness at a current density of 200 A per square meter.)

Generally, in the case of video display, the current applied to (passed through) each EL element 15 is approximately 0.2 of a white peak current (a current which flows at a rated

terminal voltage, or a current with a current density of 100 A per square meter according to examples cited herein).

Therefore, for video display in the example in Figure 45, the value of the horizontal axis should be multiplied by 0.2. Thus, the reverse bias voltage Vm and the application duration rate t1 (or t2 or the ratio between t1 and t2) should be determined in such a way as to make |reverse bias voltage × t1|/(rated terminal voltage × t2) equal to 0.2 or larger. Preferably, the reverse bias voltage Vm and the application duration rate t1 should be determined in such a way as to make |reverse bias voltage × t1|/(rated terminal voltage × t2) equal to 0.35 (= 1.75 × 0.2) or smaller.

That is, on the horizontal axis (|reverse bias voltage × t1|/(rated terminal voltage × t2)) in Figure 45, the value of 1.0 should be changed to 0.2. Thus, if video is displayed on the display panel (probably this is normally the case and white raster is not likely to be displayed constantly), the reverse bias voltage Vm should be applied for a predetermined time t1 in such a way as to make |reverse bias voltage × t1|/(rated terminal voltage × t2) equal to 0.2 or larger. Even if the value of |reverse bias voltage × t1|/(rated terminal voltage × t2) is increased, the terminal voltage ratio does not increase greatly as shown in Figure 45. Thus, an upper limit should be set to make |reverse bias voltage × t1|/(rated terminal voltage × t2) equal to 1.75 or smaller by allowing

for white raster display.

The reverse bias driving according to the present invention will be described below with reference to drawings. In a pixel configuration for reverse bias driving, an N-channel transistor 11g is used as shown in Figure 47. Of course, this may be a P-channel transistor.

In Figure 47, as the voltage applied to a gate potential control line 473 is set higher than the voltage applied to a reverse bias line 471, the transistor 11g (N) turns on and the reverse bias voltage Vm is applied to the anode electrode of the EL element 15.

In the pixel configuration in Figure 47 and the like, the gate potential control line 473 may be operated constantly at a fixed potential. For example, in Figure 47, when voltage Vk is 0 (V), the potential of the gate potential control line 473 is set to 0 (V) or higher (preferably, 2 V or higher). Incidentally, this potential is denoted by Vsg. In this state, as the potential of the reverse bias line 471 is set to the reverse bias voltage Vm (0 V or lower, and preferably -5 V or lower than Vk), the transistor 11g (N) turns on and the reverse bias voltage Vm is applied to the anode electrode of the EL element 15. As the voltage of the reverse bias line 471 is set higher than the voltage applied to the gate potential control line 473 (i.e., the gate (G) terminal voltage of the transistor 11g), the transistor 11g stays off and the reverse

bias voltage Vm is not applied to the anode electrode of the EL element 15. Of course, it goes without saying that in this state, the reverse bias line 471 may be put into a high-impedance state (such as an open state).

Also, a gate driver circuit 12c may be formed or placed separately to control the reverse bias line 471 as illustrated in Figure 48. The gate driver circuit 12c operates by shifting in sequence as in the case of the gate driver circuit 12a and the location of application of the reverse bias voltage is shifted in sync with the shift operation.

The drive method described above makes it possible to apply the reverse bias voltage Vm to the EL element 15 by varying only the potential of the reverse bias line 471 with the gate (G) terminal of the transistor 11g set at a fixed potential. This makes it easy to control the application of the reverse bias voltage Vm.

The reverse bias voltage Vm is applied when current is not passed through the EL element 15. This can be done by turning on the transistor 11g when the transistor 11d is off. That is, the reverse of on/off logic of the transistor 11d can be applied to the gate potential control line 473. For example, in Figure 47, the gate (G) terminal of the transistors 11d and 11g can be connected to the gate signal line 17b. Since the transistor 11d is a P-channel transistor and the transistor 11g is an N-channel transistor, they turn

on and off in the opposite manner.

Figure 49 is a timing chart of reverse bias driving. In the chart, the subscripts such as (1) and (2) indicate pixel row numbers. It is assumed for ease of explanation that (1) indicates the first pixel row while (2) indicates the second pixel row, but this is not restrictive. It is also possible to consider that (1) indicates the N-th pixel row while (2) indicates the (N + 1)-th pixel row. The same applies to other examples except for some special cases. Although examples in Figure 49 and the like are described by citing the pixel configuration in Figure 1 and the like, this is not restrictive. They are also applicable, for example, to the pixel configurations in Figures 41, 38, etc.

When a turn-on voltage (Vgl) is applied to the gate signal line 17a (1) in the first pixel row, a turn-off voltage (Vgh) is applied to the gate signal line 17b (1) in the first pixel row. Thus, the transistor 11d is off and current does not flow through the EL element 15.

A voltage Vsl (which turns on the transistor 11g) is applied to a reverse bias line 471(1). Thus, the transistor 11d is on and a reverse bias voltage is applied to the EL element 15. The reverse bias voltage is applied a predetermined period (1/200 of 1 H or longer; or 0.5 μsec) after the turn-off voltage (Vgh) is applied to the gate signal line 17b. The reverse bias voltage is turned off a predetermined period (1/200 of

1 H or longer; or 0.5 μsec) before the turn-on voltage (Vgl) is applied to the gate signal line 17b. This is done in order to prevent the transistors 11d and 11g from turning on simultaneously.

In the next 1 H (horizontal scanning period), a turn-off voltage (Vgh) is applied to the gate signal line 17a, and the second pixel row is selected. That is, a turn-on voltage is applied to a gate signal line 17b(2). On the other hand, a turn-on voltage (Vgl) is applied to the gate signal line 17b, the transistor 11d is turned on, and a current from the transistor 11a flows through the EL element 15, causing the EL element 15 to emit light. Also, a turn-off voltage (Vsh) is applied to the reverse bias line 471(1) stopping the reverse bias voltage from being applied to the EL elements 15 in the first pixel row (1). The voltage Vsl (reverse bias voltage) is applied to a reverse bias line 471(2) in the second pixel row.

As the above operations are repeated in sequence the images on the entire screen is rewritten. In the above example, a reverse bias voltage is applied while the pixels are being programmed. However, the circuit configuration in Figure 48 is not limited to this. It is obvious that a reverse bias voltage may be applied to a plurality of pixel rows continuously. It is also obvious that the reverse bias driving may be used in combination with block driving (see Figure 40), N-fold pulse

driving, reset driving, or dummy pixel driving.

Reverse bias voltage can be applied not only during image display.

The reverse bias voltage may be applied for a predetermined period after the EL display apparatus is turned off.

Although the above example has been described with reference to the pixel configuration in Figure 1, it goes without saying that the use of reverse bias voltage is also applicable to the pixel configurations in Figures 38 and 41 and the like. For example, Figure 50 shows a pixel configuration for current programming.

Figure 50 shows a pixel configuration of a current mirror. The transistor 11d turns on 1 H (horizontal scanning period, i.e., one pixel row) or more before the given pixel is selected. Preferably, it turns on at least 3 Hs before. In that case, the transistor 11d turns on 3 Hs before selection of the pixel, short-circuiting the gate (G) terminal and drain (D) terminal of the transistor 11a. Consequently, the transistor 11a is turned off. Thus, the current stops flowing through the transistor 11b and the EL element 15 is turned off.

When the EL element 15 is not illuminated, the transistor 11g turns on, applying a reverse bias voltage to the EL element 15. Thus, the reverse bias voltage is applied while the transistor 11d is on. Consequently, the transistor 11d and transistor 11g turn on simultaneously in logical terms.

The voltage Vsg is applied continuously to the gate (G) terminal of the transistor 11g.

The transistor 11g turns on when a reverse bias voltage sufficiently smaller than the voltage Vsg is applied to the reverse bias line 471.

Subsequently, when there comes a horizontal scanning period in which a video signal is applied to (written into) the pixel, a turn-on voltage is applied to a gate signal line 17a1, turning on the transistor 11c.

Thus, a video signal voltage outputted from the source driver circuit 14 to the source signal line 18 is applied to the capacitor 19 (the transistor 11d remains on).

When the transistor 11d is turned on, the pixel is put into black display mode.

The longer the conduction period of the transistor 11d in one field (one frame) period, the larger the proportion of the black display period. Thus, the brightness during a display period needs to be increased to obtain a desired average brightness over one field (one frame) in spite of the black display period. That is, the current to be passed through the EL element 15 during the display period needs to be increased. This operation is based on the N-fold pulse driving according to the present invention. Thus, an operation characteristic of the present invention is implemented by a combination of the N-fold pulse driving and driving which involves creating

- 212 -

a black display by turning on the transistor 11d. Also, a configuration (method) characteristic of the present invention involves applying a reverse bias voltage to the EL element 15 when the EL element 15 is not illuminated.

The N-fold pulse driving allows a predetermined current (programmed current (at a voltage held in the capacitor 19)) to be passed through the EL element 15 again during one field (one frame) period even after a black display is created once. With the configuration in Figure 50, however, once the transistor 11d turns on, since the capacitor 19 is discharged (or its charge is reduced), it is not possible to pass a predetermined current (programmed current) through the EL element 15. However, this configuration features ease of circuit operation.

Incidentally, although the above example uses a pixel configuration for current programming, the present invention is not limited to this and is applicable to other current-based pixel configurations such as those shown in Figures 38 and 50. It is also applicable to a pixel configuration for voltage programming such as the one shown in Figures 51, 54, and 62.

Figure 51 shows typically one of the simplest pixel configurations for voltage programming. The transistor 11b acts as a selection switching element while the transistor 11a acts as a driver transistor which applies current to the EL element 15. This configuration contains a transistor

(switching element) 11g which applies a reverse bias voltage to the anode of the EL element 15.

With the pixel configuration in Figure 51, the current to be passed through the EL element 15 is applied to the source signal line 18. Then, it is applied to the gate (G) terminal of the transistor 11a as the transistor 11b is selected.

To describe the configuration in Figure 51, basic operation will be described first with reference to Figure 52. The pixel configuration in Figure 51 is of a voltage offset canceling type and operates in four stages: initialization operation, reset operation, programming operation, and light-emitting operation.

The initialization operation is performed after a horizontal synchronization signal (HD) is provided. A turn-on voltage is applied to the gate signal line 17b, turning on the transistor 11g. Besides, a turn-on voltage is also applied to the gate signal line 17a, turning on the transistor 11c. At this time, a voltage Vdd is applied to the source signal line 18. Thus, the voltage Vdd is applied to a terminal a of the capacitor 19b. In this state, the driver transistor 11a turns on and a small current flows through the EL element 15. This current makes the voltage on the drain (D) terminal of the driver transistor 11a larger in absolute value than at least the voltage at an operating point of the driver transistor 11a.

Next, the reset operation is performed. A turn-off voltage is applied to the gate signal line 17b, turning off the transistor 11e. On the other hand, a turn-on voltage is applied to the gate signal line 17c for a period of T1, turning on the transistor 11b. The period T1 corresponds to a reset period. A turn-on voltage is applied to the gate signal line 17a continuously for a period of 1 H. Preferably, the period T1 is between 20% and 90% (both inclusive) of 1 H or between 20 μsec and 160 μsec (both inclusive). Preferably, a capacitance ratio Ca/Cb between a capacitor 19b (Cb) and capacitor 19a (Ca) is between 1/6 and 2/1 (both inclusive).

During a reset period, the transistor 11b turns on, short-circuiting the gate (G) terminal and drain (D) terminal of the driver transistor 11a. Thus, the voltages at the gate (G) terminal and drain (D) terminal of the transistor 11a become equal, putting the transistor 11a in an offset mode (reset mode: a state in which no current flows). In the reset mode, the voltage at the gate (G) terminal of the transistor 11a approaches a starting voltage at which a current starts to flow. A gate voltage which maintains the reset mode is held at a terminal b of the capacitor 19b. Thus, the capacitor 19 holds an offset voltage (reset voltage).

In a next programming mode, a turn-off voltage is applied to the gate signal line 17c, turning off the transistor 11b. On the other hand, DATA voltage is applied to the source signal

line 18 for a period of Td. Thus, the sum of the DATA voltage

and offset voltage (reset voltage) is applied to the gate (G)

terminal of the driver transistor 11a. This allows the driver

transistor 11a to pass a programmed current.

After the programming period, a turn-off voltage is

applied to the gate signal line 17a, turning off the transistor

11c and cutting off the driver transistor 11a from the source

signal line 18. Besides, a turn-off voltage is also applied

to the gate signal line 17c, turning off the transistor 11b,

which remains off for a period of 1F. On the other hand, a

turn-on voltage and turn-off voltage are applied to the gate

signal line 17b periodically, as required. Thus, if combined

with N-fold pulse driving in Figures 13, 15, etc. or with

interlaced driving, this method can achieve even better image

display.

With the drive system in Figure 52, in reset mode, the

capacitor 19 holds a starting current voltage (offset voltage,

reset voltage) of the transistor 11a. Thus, the darkest black

display is created when the reset voltage is being applied

to the gate (G) terminal of the driver transistor 11a.

However, coupling between the source signal line 18 and pixel

16, penetration voltage to the capacitor 19, or punch-through

of a transistor causes excessive brightness (reduced contrast)

resulting in a whitish screen. Therefore, the drive method

described with reference to Figure 53 cannot achieve high

display contrast.

To apply the reverse bias voltage Vm to the EL element 15, it is necessary to turn off the transistor 11a. To turn off the transistor 11a, the Vdd terminal and gate (G) terminal of the transistor 11a can be short-circuited. This configuration will be described with reference to Figure 53 later.

Alternatively, it is possible to apply the Vdd voltage or a voltage which turns off the transistor 11a to the source signal line 18, turn on the transistor 11b, and apply the voltage to the gate (G) terminal of the transistor 11a. This voltage turns off the transistor 11a (or makes it pass almost no current (almost off: the transistor 11a is in a high-impedance state)). Subsequently, the transistor 11g is turned on and a reverse bias voltage is applied to the EL element 15.

Next, reset driving in the pixel configuration in Figure 51 will be described. Figure 53 shows an example. As shown in Figure 53, the gate signal line 17a connected to the gate (G) terminal of the transistor 11c in a pixel 16a is also connected to the gate (G) terminal of the reset transistor 11b in a pixel 16b in the next stage. Similarly, the gate signal line 17a connected to the gate (G) terminal of the transistor 11c in the pixel 16b is also connected to the gate (G) terminal of the reset transistor 11b in a pixel 16c in the next stage.

Thus, when a turn-on voltage is applied to the gate signal line 17a connected to the gate (G) terminal of the transistor 11c in the pixel 16a, the pixel 16a enters voltage programming mode, the reset transistor 11b of the pixel 16b in the next stage turns on, and the driver transistor 11a of the pixel 16b is reset. Similarly, when a turn-on voltage is applied to the gate signal line 17a connected to the gate (G) terminal of the transistor 11c in the pixel 16b, the pixel 16b enters current programming mode, the reset transistor 11b of the pixel 16c in the next stage turns on, and the driver transistor 11a of the pixel 16c is reset. Thus, reset driving by way of a preceding-stage gate control system can be implemented easily. Also, the number of leads from a gate signal line per pixel can be reduced.

More detailed description will be provided. Suppose voltage is applied to gate signal lines 17 as shown in figure 53(a). Specifically, a turn-on voltage is applied to the gate signal line 17a of the pixel 16a and a turn-off voltage is applied to the gate signal lines 17a of other pixels 16. Also, a turn-off voltage is applied to the gate signal lines 17b of the pixels 16a and 16b while a turn-on voltage is applied to the gate signal lines 17b of the pixels 16c and 16d.

In this state, the pixel 16a is in voltage programming mode and is not illuminated, the pixel 16b is in reset mode and not illuminated, the pixel 16c is pending current

programming and is illuminated, and the pixel 16d is pending current programming and is illuminated.

After 1 H, data in a shift register 61 circuit of the controlling gate driver circuit 12 is shifted one bit to enter a state shown in Figure 53(b). In Figure 53(b), the pixel 16a is pending current programming and is illuminated, the pixel 16b is current programming mode and is not illuminated, the pixel 16c is in reset mode and is not illuminated, and the pixel 16d is pending programming and is illuminated.

Thus, it can be seen that the voltage applied to the gate signal line 17a of each pixel resets the driver transistor 11a of the pixel in the next stage to perform voltage programming in the next horizontal scanning period sequentially.

The pixel configuration for voltage programming in Figure 43 can also implement preceding-stage gate control. Figure 54 shows an example in which a connection method of a preceding-stage gate control system is used for the pixel configuration in Figure 43.

In Figure 54, the gate signal line 17a connected to the gate (G) terminal of the transistor 11b in the pixel 16a is connected to the gate (G) terminal of the reset transistor 11e in the pixel 16b in the next stage.
Similarly, the gate signal line 17a connected to the gate (G) terminal of the transistor 11b in the pixel 16b is connected to the gate (G) terminal of the reset transistor 11e in the

pixel 16c in the next stage.

Thus, when a turn-on voltage is applied to the gate signal line 17a connected to the gate (G) terminal of the transistor 11b in the pixel 16a, the pixel 16a enters voltage programming mode, the reset transistor 11e of the pixel 16b in the next stage turns on, and the driver transistor 11a of the pixel 16b is reset. Similarly, when a turn-on voltage is applied to the gate signal line 17a connected to the gate (G) terminal of the transistor 11b in the pixel 16b, the pixel 16b enters current programming mode, the reset transistor 11e of the pixel 16c in the next stage turns on, and the driver transistor 11a of the pixel 16c is reset. Thus, reset driving by way of a preceding-stage gate control system can be implemented easily.

More detailed description will be provided. Suppose voltage is applied to gate signal lines 17 as shown in figure 55(a). Specifically, a turn-on voltage is applied to the gate signal line 17a of the pixel 16a and a turn-off voltage is applied to the gate signal lines 17a of other pixels 16. It is assumed that all the transistors 11g for reverse biasing are off.

In this state, the pixel 16a is in voltage programming mode, the pixel 16b is in reset mode, the pixel 16c is pending current programming, and the pixel 16d is pending current programming.

After 1 H, data in the shift register 61 circuit of the

controlling gate driver circuit 12 is shifted one bit to enter a state shown in Figure 55(b). In Figure 55(b), the pixel 16a is pending current programming, the pixel 16b is in current programming mode, the pixel 16c is in reset mode, and the pixel 16d is pending programming.

Thus, it can be seen that the voltage applied to the previous stage for the gate signal line 17a of each pixel resets the driver transistor 11a of the pixel in the next stage to perform voltage programming in the next horizontal scanning period sequentially.

For completely black display in current driving, the driver transistors 11 of the pixels are programmed with 0 current. That is, the source driver circuit 14 delivers no current. When no current is delivered, parasitic capacitance caused in the source signal line 18 cannot be discharged and the potential of the source signal line 18 cannot be varied. Consequently, the gate potential of the driver transistors also remains unchanged and the potential in the previous frame (field) (1 F) remains accumulated in the capacitor 19. For example, if the previous frame contains white display, the white display is retained even if the current frame contains completely black display.

To solve this problem, according to the present invention, a black level voltage is written into the source signal line 18 at the beginning of one horizontal scanning period (1 H)

before the current to be programmed is output to the source signal line 18. For example, if image data consists of the 0th to 7th gradations close to black level, a black level voltage is written only during a certain period at the beginning of one horizontal scanning period to reduce the load of current programming and make up for insufficient writing. Incidentally, completely black display corresponds to the 0th gradation and white display corresponds to the 63rd gradation (in the case of 64-gradation display). Precharging will be described in detail later.

The current-driven source driver IC (circuit) 14 according to the present invention will be described below. The source driver IC according to the present invention is used to implement the drive methods and drive circuits according to the present invention described earlier. It is used in combination with drive methods, drive circuits, and display apparatus according to the present invention. Incidentally, although the source driver circuit will be described as an IC chip, this is not restrictive and the source driver circuit may be built on the display panel using low-temperature polysilicon technology, or the like.

First, an example of a conventional current-driven source driver circuit is shown in Figure 72, which provides a principle needed to describe current-driven source driver IC (source driver circuit) according to the present invention.

In Figure 72, reference numeral 721 denotes a D/A converter. The D/A converter 721 is fed an n-bit data signal and outputs an analog signal based on the inputted data. The analog signal enters an operational amplifier 722, which feeds into an N-channel transistor 631a. Current flowing through the N-channel transistor 631a flows to a resister 691. A terminal voltage of the register R provides a negative input to the operational amplifier 722. The voltage at the negative terminal equals the voltage at the positive terminal of the operational amplifier 722. Thus, the output voltage of the D/A converter 721 equals the terminal voltage of the resister 691.

If the resistance of the resister 691 is 1 MΩ and the output of the D/A converter 721 is 1 (V), a current of 1 (V)/1 MΩ = 1 (μA) flows through the resister 691, forming a constant current circuit. Thus, analog output of the D/A converter 721 varies with the value of data signal, and a predetermined current flows through the resister 691 according to the analog output to provide a programming current Iw.

However, the D/A converter circuit 721 has a large circuit scale. So does the operational amplifier 722. Formation of the D/A converter circuit 721 and operational amplifier 722 in a single output circuit results in a huge source driver IC 14, which is practically impossible to build.

The present invention has been made in view of the above point. The source driver circuit 14 according to the present invention has a circuit configuration and layout configuration which reduces the scale of a current output circuit and minimizes variations in output current among current output terminals.

Figure 63 is a block diagram showing a current-driven source driver IC (circuit) 14 according to the present invention. Figure 63 shows a multi-stage current mirror circuit comprising three-stage current sources (631, 632, 633).

In Figure 63, the current value of the current source 631 in the first stage is copied by the current mirror circuit to N current sources 632 in the second stage (where N is an arbitrary integer). The current values of the second-stage current sources 632 are copied by the current mirror circuit to M current sources 633 in the third stage (where M is an arbitrary integer). Consequently, this configuration causes the current value of the first-stage current source 631 to be copied to N × M third-stage current sources 633.

For example, when driving the source signal lines 18 with one driver IC 14, there are 176 outputs (because the source signal lines require a total of 176 outputs for R, G, and B). Here it is assumed that N = 16 and M = 11. Thus, 16 × 11 = 176 and the 176 outputs can be covered. In this way, by using

a multiple of 8 or 16 for N or M, it becomes easier to lay out and design the current sources of the driver IC.

The current-driven source driver IC (circuit) 14 employing the multi-stage current mirror circuit according to the present invention can absorb variations in transistor characteristics because it has the second-stage current sources 632 in between instead of copying the current value of the first-stage current source 631 directly to N × M third-stage current sources 633 using the current mirror circuit.

In particular, the present invention is characterized in that a first-stage current mirror circuit (current source 631) and second-stage current mirror circuits (current sources 632) are placed close to each other. If a first-stage current source 631 are connected with third-stage current sources 633 (i.e., in the case of two-stage current mirror circuit), the second-stage current sources 633 connected to the first-stage current source are large in number, making it impossible to place the first-stage current source 631 and third-stage current sources 633 close to each other.

The source driver circuit 14 according to the present invention copies the current value of the first-stage current mirror circuit (current source 631) to the second-stage current mirror circuits (current sources 632), and the current values of the second-stage current mirror circuits (current sources

632) to the third-stage current mirror circuits (current
sources 632). With this configuration, the second-stage
current mirror circuits (current sources 632) connected to
the first-stage current mirror circuit (current source 631)
are small in number. Thus, the first-stage current mirror
circuit (current source 631) and second-stage current mirror
circuits (current sources 632) can be placed close to each
other.

If transistors composing the current mirror circuits can
be placed close to each other, naturally variations in the
transistors are reduced, and so are variations in current
values. The number of the third-stage current mirror circuits
(current sources 633) connected to the second-stage current
mirror circuits (current sources 632) are reduced as well.
Consequently, the second-stage current mirror circuits
(current sources 632) and third-stage current mirror circuits
(current sources 633) can be placed close to each other.

That is, transistors in current receiving parts of the
first-stage current mirror circuit (current source 631),
second-stage current mirror circuits (current sources 632),
and third-stage current mirror circuits (current sources 633)
can be placed close to each other on the whole. In this way,
transistors composing the current mirror circuits can be placed
close to each other, reducing variations in the transistors
and greatly reducing variations in current signals from output

terminals. A multi-stage current mirror circuit consisting of three stages has been cited in the above example for the sake of simplicity. Needless to say, the larger the number of stages, the smaller the current variations in the source driver IC 14 of the current-driven display panel.
Thus, the number of stages of a current mirror circuit is not limited to three and may be more than three.

In the present invention, the terms "current sources 631, 632, and 633" and "current mirror circuits" are used interchangeably. That is, current sources are a basic construct of the present invention and the current sources are embodied into current mirror circuits. Thus, a current source is not limited to a current mirror circuit and may be a current circuit consisting of a combination of a operational amplifier 722, transistor 631, and register R as shown in Figure 72.

Figure 64 is a structural drawing of a more concrete source driver IC (circuit) 14. It illustrates part of third current sources 633. This is an output part connected to one source signal line 18. It is composed of multiple current mirror circuits (current sources 634 (1 unit)) of the same size as a current mirror configuration in the final stage. Their number is bit-weighted according to the data size of image data.

Incidentally, the transistors composing the source driver IC (circuit) 14 according to the present invention are not limited to a MOS type and may be a bipolar type. Also, they are not limited to silicon semiconductors and may be gallium arsenide semiconductors. Also, they may be germanium semiconductors. Alternatively, they may be formed directly on a substrate using low-temperature polysilicon technology, other polysilicon technology, or amorphous silicon technology.

Figure 48 illustrates an example of the present invention which handles 6-bit digital input. Six bits are the sixth power of two, and thus provide a 64-gradation display. This source driver IC 14, when mounted on an array board, provides 64 gradations each of red (R), green (G), and blue (B), meaning 64 × 64 × 64 = approximately 260,000 colors.

Sixty-four (64) gradations require one D0-bit unit transistor 634, two D1-bit unit transistors 634, four D2-bit unit transistors 634, eight D3-bit unit transistors 634, sixteen D4-bit unit transistors 634, and thirty-two D5-bit unit transistors 634 for a total of sixty-three unit transistors 634. Thus, the present invention produces one output using as many unit transistors 634 as the number of gradations (64 gradations in this example) minus 1. Incidentally, even if one unit transistor is divided into a plurality of sub-unit transistors, this simply means that a

unit transistor is divided into sub-unit transistors, and makes no difference in the fact that the present invention uses as many unit transistors as the number of gradations minus 1.

In Figure 64, D0 represents LSB input and D5 represents MSB input. When a D0 input terminal is high (positive logic), a switch 641a is closed (the switch 481a is an on/off means and may be constructed of a single transistor or may be an analog switch consisting of a P-channel transistor and N-channel transistor. Then, current flows to a current source (single-unit) 634 composing a current mirror. The current flows through internal wiring 643 in the IC 14. Since the internal wiring 643 is connected to the source signal line 18 via a terminal electrode of the IC 14, the current flowing through internal wiring 643 provides a programming current for the pixels 16.

For example, when a D1 input terminal is high (positive logic), a switch 641b is closed. Then, current flows to two current sources (single-unit) 634 composing a current mirror. The current flows through the internal wiring 643 in the IC 14. Since the internal wiring 643 is connected to the source signal line 18 via a terminal electrode of the IC 14, the current flowing through internal wiring 643 provides a programming current for the pixels 16.

The same applies to the other switches 641. When a D2 input terminal is high (positive logic), a switch 641c is closed.

Then, current flows to four current sources (single-unit) 634 composing a current mirror. When a D5 input terminal is high (positive logic), a switch 641f is closed. Then, current flows to 32 (thirty-two) current sources (single-unit) 634 composing a current mirror.

In this way, based on external data (D0 to D5), current flows to the corresponding current sources (single-unit). That is, current flows to 0 to 63 current sources (single-unit) depending on the data.

Incidentally, for ease of explanation, it is assumed that there are 63 current sources for a 6-bit configuration, but this is not restrictive. In the case of 8-bit configuration, 255 unit transistors 634 can be formed (placed). For a 4-bit configuration, 15 unit transistors 634 can be formed (placed). The transistors 634 constituting the unit current sources have a channel width W and channel width L. The use of equal transistors makes it possible to construct output stages with small variations.

Besides, not all the current sources 634 need to pass equal current. For example, individual current sources 634 may be weighted. For example a current output circuit may be constructed using a mixture of single-unit current sources 634, double-sized current sources 634, quadruple-sized current sources 634, etc. However, if current sources 634 are weighted, the weighted current sources may not provide

the right proportions, resulting in variations. Thus, even when using weighting, it is preferable to construct each current source from transistors each of which corresponds to a single-unit current source.

The unit transistor 634 should be equal to or larger than a certain size. The smaller the transistor size, the larger the variations in output current. The size of a transistor 634 is given by the channel length L multiplied by the channel width W. For example, if $W = 3$ μm and $L = 4$ μm, the size of the unit transistor 634 constituting a unit current source is $W \times L = 12$ square μm. It is believed that crystal boundary conditions of silicon wafers have something to do with the fact that a smaller transistor size results in larger variations. Thus, variations in output current of transistors are small when each transistor is formed across a plurality of crystal boundaries.

Relationship between size of transistors and variations in output current is shown in Figure 117. The horizontal axis of the graph in Figure 117 represents transistor size (square μm). The vertical axis represents variations in output current in percentage terms. The variations (%) in output current here were determined using groups of 63 unit current sources (unit transistors) 634 formed on a wafer. Thus, although the horizontal axis of the graph represents the size of a transistor constituting one current source, since there

are actually 63 transistors connected in parallel, the total area of the transistors is 63 times larger. However, the present invention is based on the size of a unit transistor 634. Thus, Figure 117 shows that variations in the output current of 63 unit transistors 634 with an area of 30 square μm each is 0.5%.

In the case of 64 gradations, 100/64 = 1.5%. Thus, the variations in the output current must be within 1.5%. From Figure 117, it can been seen that in order for the variations to be within 1.5%, the size of the unit transistor must be equal to or larger than 2 square μm (in the case of 64 gradations, sixty-three 2-square μm unit transistors operate). On the other hand, there are limits to transistor size because larger transistors increase the size of an IC chip and there are limits to the width per one output. In this respect, the upper limit to the size of the unit transistor 634 is 300 square μm. Thus, in the case of 64 gradations, the size of the unit transistor 634 must be from 2 square μm to 300 square μm (both inclusive).

In the case of 128 gradations, 100/128 = 1%. Thus, the variations in the output current must be within 1%. From Figure 117, it can been seen that in order for the variations to be within 1%, the size of the unit transistor must be equal to or larger than 8 square μm. Thus, in the case of 128 gradations, the size of the unit transistor 634 must be from 8 square μm to 300 square μm (both inclusive).

Generally, if the number of gradations is K and the size of a unit transistor 634 is St (square μm), the following relationship should be satisfied:

$40 \leq K/\sqrt{(St)}$ and $St \leq 300$

More preferably, the following relationship should be satisfied:

$120 \leq K/\sqrt{(St)}$ and $St \leq 300$

In the above example 64 gradations are represented by 63 transistors. When representing 64 gradations by 127 unit transistors 634, the unit-transistor 634 size is the total size of two unit transistors 634. For example, in the case where 64 gradations are represented by 127 unit transistors 634, if the size of a unit transistor 484 is 10 square μm, the unit-transistor 484 size is given in Figure 117 as 10 × 2 = 20. Similarly, in the case where 64 gradations are represented by 255 unit transistors 634, if the size of a unit transistor 484 is 10 square μm, the unit-transistor size is given in Figure 117 as 10 × 4 = 40.

It is necessary to take into consideration not only the size, but also the shape of the unit transistor 634. This is to reduce kink effect. A kink is a phenomenon in which current flowing through a unit transistor 634 changes when the voltage between the source (S) and drain (D) of the unit transistor 634 is varied with the gate voltage of the unit transistor 634 kept constant. In the absence of kink effect

(in ideal state), the current flowing through the unit transistor 634 does not change even if the voltage applied between the source (S) and drain (D) of the unit transistor 484 is varied.

Kink effect occurs when the source signal lines 18 vary due to variations in Vt of driver transistors 11a shown in Figure 1 and the like. The driver circuit 14 passes programming current through the source signal line 18 so that the programming current will flow through the driver transistor 11a of the pixel. The programming current causes changes in the gate terminal voltage of the driver transistor 11a, and consequently the programming current flows through the driver transistor 11a. As can be seen From Figure 3, when a selected pixel 16 is in programming mode, the gate terminal voltage of the driver transistor 11a equals the potential of the source signal line 18.

Thus, the potentials of the source signal lines 18 vary due to variations in Vt of the driver transistors 11a in pixels 16. The potential of a source signal line 18 equals the source-drain voltage of the unit transistor 634 of the driver circuit 14. That is, variations in Vt of the driver transistors 11a in the pixels 16 cause the source-drain voltage applied to the unit transistors 634 to vary. Then, the source-drain voltage causes variations in the output voltage of the unit transistor 634 due to kinks.

Figure 118 is a graph which represents this phenomenon. The vertical axis represents the output current of the unit transistor 634 obtained when a predetermined voltage is applied to the gate terminal. The horizontal axis represents the voltage between source (S) and drain (D). L in L/W represents the channel length and W represents the channel width of the unit transistor 634. Also, L, W represents the size of the unit transistor 634 which outputs current for one gradation. Thus, to output with the current for one gradation using a plurality of sub-unit transistors, W and L should be calculated by substituting the sub-unit transistors with an equivalent unit transistor 634. Basically, the calculation should be performed by taking into consideration the transistor size and output current.

When L/W equals 5/3, the output current remains almost unchanged even if the source-drain voltage rises. However, when L/W equals 1/1, the output current increases in approximate proportion to the source-drain voltage. Thus, the larger the L/W, the better.

Figure 172 is a graph showing deviation (variation) in L/W of unit transistors from a target value. When the L/W ratio of unit transistors is equal to smaller than 2, the deviation from the target value is large (the slope of the straight line is large). However, as L/W increases, the deviation from the target value tends to decrease. When L/W

of unit transistors is equal to larger than 2, the deviation
from the target value is small. Also, the deviation from the
target value is 0.5% or less when L/W = 2 or more. Thus, this
value can be used for source driver circuits 14 to indicate
accuracy of transistors.

In view of the above circumstances, it is preferable that
L/W of a unit transistor is two or more.

However, a large L/W means a long L, and thus a large
transistor size.

Thus, more preferably, L/W is 40 or less.

Besides, L/W also depends on the number of gradations.
If the number of gradations is small, there is no problem even
if there are variations in the output current of the unit
transistor 634 due to kink effect because there are large
differences between gradations. However, in the case of a
display panel with a large number of gradations, since there
are small differences between gradations, even small
variations in the output current of the unit transistor 634
due to kink effect will decrease the number of gradations.

In view of the above circumstances, the driver circuit
14 according to the present invention is configured to satisfy
the following relationship:

$(\sqrt{(K/16)}) \leq L/W \leq$ and $(\sqrt{(K/16)}) \times 20$

where K is the number of gradations, L is the channel length
of the unit transistor 634, and W is the channel width of the

unit transistor. This relationship is illustrated in Figure 119. The area above the straight line in Figure 119 is relevant to the present invention.

This corresponds to the third-stage current mirror portion illustrated in Figure 63. Thus, a first current source 631 and second current sources 632 are formed separately and are placed densely (close to each other). Besides, the transistors 633a in the current mirror circuits composing the second current sources 632 and third current sources are also placed densely (close to each other).

The variations in the output current of the unit transistor 634 also depend on the voltage resistance of the source driver IC 14. The voltage resistance of the source driver IC generally means the power supply voltage of the IC. For example, voltage resistance of 5 V means the use of the power supply voltage at a standard voltage of 5 V. Incidentally, IC voltage resistance can translate into maximum working voltage. Semiconductor IC makers have standardized voltage-resistance processes such as a 5-V voltage-resistance process and 10-V voltage-resistance process.

It is believed that film properties and film thickness of a gate insulating film of the unit transistor 634 have something to do with the fact that IC voltage resistance affects variations in the output current of the unit transistor 634. The transistors 634 produced in a process with high IC voltage

resistance have a thick gate insulating film. This is intended to avoid dielectric breakdown even under application of a high voltage. A thick gate insulating film makes its control difficult and increases variations in its film properties. This increases variations in the transistors. Also, the transistors produced in a high voltage-resistance process have low mobility. With low mobility, even slight changes in electrons injected into transistor gates cause changes in characteristics. This increases variations in the transistors. To reduce variations in the unit transistors 634, it is preferable to adopt an IC process with low IC voltage resistance.

Figure 170 illustrates relationship between IC voltage resistance and output variations of unit transistors. The variation rate on the vertical axis is based on the variation of unit transistors 634 produced in a 1.8-V voltage resistance process, which variation is taken to be 1. Figure 170 shows output variations of unit transistors 634 which were produced in various IC voltage resistance processes and have a shape of L/W = 12/6 (μm). A plurality of unit transistors 634 were produced in each IC voltage resistance process and variations in their output current were determined. The voltage resistance processes were composed discretely of 1.8-V voltage resistance, 2.5-V voltage resistance, 3.3-V voltage resistance, 5-V voltage resistance, 8-V voltage resistance,

and 10-V voltage resistance, 15-V voltage resistance processes. However, for ease of explanation, variations in the transistors formed in the different voltage resistance processes are plotted on the graph and connected with straight lines.

As can be seen from Figure 170, the variation rate (variations in the output current of the unit transistors 634) increases gradually up until an IC voltage resistance of 9 V. However, when the IC voltage resistance exceeds 10 V, the slope of the variation rate with respect to the IC voltage resistance becomes large.

In Figure 170, the permissible limit to the variation rate is 3 for 64- to 256-gradation display. The variation rate varies with the area, L/W, etc. of the unit transistor 634. However, the variation rate with respect to the IC voltage resistance is hardly affected by the shape of the unit transistor 634. The variation rate tends to increase above an IC voltage resistance of 9 to 10 V.

On the other hand, the potential at an output terminal 64 in Figure 64 varies with the programming current in the driver transistor 11a of the pixel 16. When the driver transistor 11a of the pixel 16 passes white raster (maximum white display) current, its gate terminal voltage is designated as Vw. When the driver transistor 11a of the pixel 16 passes black raster (completely black display) current, its gate terminal voltage is designated as Vb. The absolute value of

Vw - Vb must be 2 V or larger.   When the voltage Vw is applied
to the output terminal 761, inter-channel voltage of the unit
transistor 634 must be 0.5 V or higher.

Thus, a voltage of 0.5 V to ((Vw - Vb) + 0.5) V is applied
to the terminal 761 (during current programming, the gate
terminal voltage of the driver transistor 11a of the pixel
16 is applied to the output terminal 761, which is connected
with the source signal line 18).   Since Vw - Vb equals 2 V,
a voltage of up to 2 V + 0.5 V = 2.5 V is applied to the output
terminal 761.   Thus, even if the output voltage (current) of
the source driver IC 14 is based on a rail-to-rail output,
the IC voltage resistance must be 2.5 V.   The amplitude required
by a terminal 741 is 2.5 V or more.

Thus, it is preferable to use a voltage resistance process
in the range of 2.5-V to 10-V (both inclusive) for the source
driver IC 14.   More preferably, a voltage resistance process
in the range of 3-V to 9-V (both inclusive) is used for the
source driver IC 14.

Incidentally, it has been described that a voltage
resistance process in the range of 2.5-V to 10-V (both
inclusive) is used for the source driver IC 12.   This voltage
resistance is also applied to examples (e.g., a low-temperature
polysilicon process) in which the source driver circuit 14
is formed directly on an array board 71. Working voltage
resistance of a source driver circuit 14 formed directly on

an array board 71 can be high and exceeds 15 V in some cases. In such cases, the power supply voltage used for the source driver circuit 14 may be substituted with the IC voltage resistance illustrated in Figure 170. Also, the source driver IC 14 may have the IC voltage resistance substituted with the power supply voltage used.

The area of a unit transistor 634 is correlated with the variations in its output current. Figure 171 is a graph obtained by varying the transistor width W of a unit transistor 634 with the area of the unit transistor 634 kept constant. In Figure 170, the variation of the unit transistor 634 with a channel width W of 2 μm is taken as 1. As can be seen from Figure 171 the variation rate increases gradually when W of the unit transistor is from 2 μm to 9 or 10 μm. The increase in the variation rate tends to become large when W is 10 μm or more. Also, the variation rate tends to increase when the channel width W = 2 μm or less.

In Figure 171, the permissible limit to the variation rate is 3 for 64- to 256-gradation display. The variation rate varies with the area of the unit transistor 634. However, the variation rate with respect to the IC voltage resistance is hardly affected by the area of the unit transistor 634.

Thus, preferably, the channel width W of the unit transistor 634 is from 2 μm to 10 μm (both inclusive). More

preferably, the channel width W of the unit transistor 634 is from 2 μm to 9 μm (both inclusive).

As illustrated in Figure 68, current flowing through second-stage current mirror circuits 632b is copied to transistors 633a which compose third-stage current mirror circuits. If a current mirror ratio is 1, the current flows through transistors 633b. The current is copied to the unit transistor 634 in the final stage.

D0, which is provided by one unit transistor 634, provides the value of the current flowing through the unit transistor 633 of the final-stage current source. D1, which is provided by two unit transistors 634, provides a two times larger current value than the final-stage current source. D2, which is provided by four unit transistors 634, provides a four times larger current value than the final-stage current source; and D5, which is provided by 32 unit transistors 484, provides a 32 times larger current value than the final-stage current source.

Accordingly, programming current Iw is output (drawn) to the source signal line via switches controlled by 6-bit image data consisting of D0, D1, D2, ..., and D5. Thus, according to activation and deactivation of the 6-bit image data consisting of D0, D1, D2, ..., and D5, currents 1 time, 2 times, 4 times, ... and/or 32 times as large as the final-stage current source 633 are added and outputted to the output line.

That is, according to activation and deactivation of the 6-bit image data consisting of D0, D1, D2, ..., and D5, 0 to 63 times as large a current as the final-stage current source 633 is output from the output line (the current is drawn from the source signal line 18).

Actually, as illustrated in Figure 146, in the source driver IC 14, reference currents (IaR, IaG, and IaB) for R, G, and B, respectively, can be adjusted by variable resistors 651 (651R, 651G, and 651B). By adjusting the reference currents Ia, the white balance can be adjusted easily.

The use of integral multiples of the current values of the final-stage current sources 633 thus makes it possible to control current values more accurately (reduce output variations among terminals) than conventional methods which use W/L-based proportional allotments.

However, this configuration is available only when the driver transistors 11a of pixels 16 are P-channel transistors and the current sources (single-unit transistors) 634 of the source driver IC 14 are N-channel transistors.
In other cases (e.g., when the driver transistors 11a of pixels 16 are N-channel transistors), the present invention can use a configuration in which the programming current Iw is a discharge current.

Now, a reference current generator circuit will be described in detail. Current output mode used for the source

driver circuit (IC) 14 of the present invention uses a reference current and outputs the programming current Iw by combining unit currents which are proportional to a reference current (source drivers of liquid crystal display panels use voltage output mode, which uses steps of voltage as signals). Figure 144 shows an example. In Figures 67, 68, 76, etc. a variable resistor 651 is used to generate reference current. In Figure 144, the variable resistor 651 in Figure 68 is replaced by the transistor 631a and current flowing through a transistor 1444 which forms a current mirror circuit in conjunction with the transistor 631a is controlled by an operational amplifier 722 or the like. The transistor 1444 and transistor 631a forms the current mirror circuit. If the current mirror factor is 1, the current flowing through the transistor 1444 provides a reference current.

Output voltage of the operational amplifier 722 is fed to an N-channel transistor 1443 and the current flowing through the N-channel transistor 1443 flows through an external resistor 691. Incidentally, a resistor 691a is a fixed-chip resister. Basically, the resistor 691a is enough. A resistor 691b is a resistive element such as a posistor or thermistor whose value changes with temperature. The resistor 691a is used to compensate for temperature characteristics of the EL element 15. The resistor 691a is inserted or placed in parallel or series with the resistor

691b according to (to compensate for) the temperature characteristics of the EL element 15. Incidentally, for ease of explanation, the resistor 691a and resistor 691b will be treated below as one resistor 691.

A resistor 691 with an accuracy of 1% or better is easily available. The resistor 691 may be built into the source driver IC 14 using diffused resistor technology or a polysilicon pattern. The chip resistor 691 is mounted on an input terminal 761a. In the case of EL display panels, in particular, the temperature characteristics of EL elements 15 differ among R, G, and B. Thus, three external resistors 691 are required for R, G, and B.

Terminal voltage of the resistor 691 provides a negative input to the operational amplifier 722 and the voltage at the negative terminal has the same magnitude as the voltage at a positive terminal of the operational amplifier 722. Thus, if a positive input voltage of the operational amplifier 722 is V1, the current obtained by dividing with this voltage by the resistance 691 flows through the transistor 1444. This current serves as the reference current. If the resistance of the resistor 691 is 100 KΩ and the input voltage of the positive terminal of the operational amplifier 722 is V1 = 1 (V), a reference current of 10 (μA) (= 1 (V)/100 KΩ) flows through the resistor 691. Preferably, the reference current is set between 2 μA and 30 μA (both inclusive).

More preferably, it is set between 5 μA and 20 μA (both inclusive). A small reference current flowing through the parent transistor 63 lowers the accuracy of the unit current source 634. Too large a reference current increases the current mirror factor converted (in the downward direction in this case) within the IC, increasing variations in the current mirror circuit, and thus lowering the accuracy of the unit current source 634 again.

The above configuration makes it possible to form an extremely accurate reference current (in terms of size and variations) provided that the positive input terminal of the operational amplifier 722 and the resistor 691 are accurate enough. When building the resistor 691 into the source driver circuit (IC) 14, it is recommended to trim the incorporated resistor to increase accuracy.

A reference voltage Vref received from a reference voltage circuit 1441 is applied to the positive terminal of the operational amplifier 722. Regarding ICs for the reference voltage circuit 1441 which outputs the reference voltage, various types are available from Maxim and other companies. Alternatively, the reference voltage Vref may be generated within the source driver circuit 14 (internally generated reference voltage Vref). Preferably, the reference voltage Vref ranges between 2 (V) and the anode voltage Vdd (V) (both inclusive).

The reference voltage is fed through a connection terminal 761a. Basically, the voltage Vref can be fed into the positive terminal of the operational amplifier 722. An electronic regulator circuit 561 is placed between the connection terminal 761a and positive terminal because the luminous efficiency of the EL elements 15 varies among R, G, and B. In other words, the electronic regulator circuit 561 is intended to adjust the current passed through each of the EL elements 15 for R, G, and B, and thereby achieve a white balance. Of course, what can be adjusted by the resistor 691 does not need to be adjusted by the electronic regulator circuit 561. For example, a variable resistor may be used as the resistor 691. One of the uses of the electronic regulator circuit 561 is to readjust white balance when the degradation rate of the EL elements 15 varies among R, G, and B. The EL elements 15 for B are especially prone to degradation. Thus, the EL elements 15 for B become darker with years of use of a EL display panel, turning the screen yellowish. In that case, the white balance is adjusted using the electronic regulator circuit 561 for B. Of course, brightness correction or white balance correction of the EL elements may be performed by linking the electronic regulator circuit 561 to a temperature sensor 781 (see Figure 78 and its description).

The electronic regulator circuit 561 is built into the IC (circuit) 14. Alternatively, it is formed directly on an

array board 71 using the low-temperature poly-silicon technology. A plurality of unit resistors (R1, R2, R3, R4, ... Rn) formed through polysilicon patterning are connected in series. Analog switches (S1, S2, S2, ... Sn+1) are placed among the unit resistors, the reference voltage Vref is divided, and the resulting voltages are output.

In Figure 148 and the like, the transistor 1443 is illustrated as a bipolar transistor, but this is not restrictive. It may be a FET or MOS transistor. Needless to say, there is no need to built the transistor 1443 into the IC 14, and may be placed outside the IC. Also, power generator and other generator circuits as well as the transistor 1443 may be built into the gate driver circuit 12.

In order to achieve full-color display on an EL display panel, it is necessary to provide a reference current for each of R, G, and B. The white balance can be adjusted by controlling the ratios of the RGB reference currents. In the case of current driving as well as the present invention, the value of current passed by the unit current source 634 is determined based on one reference current. Thus, the current passed by the unit current source 634 can be determined by determining the magnitude of the reference current. Consequently, the white balance in every gradation can be achieved by setting a reference current for each of R, G, and B. The above matters work because the source driver circuit 14 produces current

outputs varied in steps (is current-driven). Thus, the point is how the magnitude of the reference current can be set for each of R, G, and B.

The light emission efficiency of an EL element is determined by, or depends heavily on, the thickness of a film vapor-deposited or applied to the EL element. The film thickness is almost constant within each lot. Through lot control of the film thickness of the EL element 15, it is possible to determine relationship between the current passed through the EL element 15 and light emission efficiency. That is, the current value used for white balancing is fixed for each lot.

For example, if the currents passed through the EL elements 15 for R, G, and B are Ir (A), Ig (A), and Ib (A), respectively, a ratio of reference currents which can achieve a white balance can be known on a lot-by-lot basis.
Therefore, a white balance can be achieved, for example, when Ir : Ig : Ib = 1 : 2 : 4. With the duty ratio driving, etc. according to the present invention, once a white balance is achieved, it is applied to all gradations. This is accomplished by synergy between a drive method according to the present invention and source driver circuit according to the present invention.

With the configuration shown in Figure 148, the values of the resistors 691 in the circuits which generate RGB

reference currents can be changed on a lot-by-lot basis to achieve a white balance. However, the resistors 691 must be changed on a lot-by-lot basis.

In Figure 148, the electronic regulator circuit 561 is controlled from the outside of the source driver circuit (IC) 14 and the value of the reference current Ia is changed by operating switches Sx in the electronic regulator circuit 561. In Figure 149, settings of the electronic regulator circuits 561 can be stored in flash memories 1491. Values in the flash memories 1491 can be set by the RGB electronic regulator circuits 561 independently of one another. The values in the flash memories 1491 are set, for example, for each lot of EL display panels and read out upon power-up of the source driver IC 14 to set the switches Sx in the electronic regulator circuits 561.

Figure 150 is a block diagram in which the electronic regulator circuit 561 in Figure 149 is configured as a resistor array circuit 1501. In Figure 150, reference character Rr denotes an external resistor. Of course, Rr may be built into the source driver circuit (IC) 14. Resistor arrays 1503 are built into the source driver circuit (IC) 14. Resistors (R1 to Rn) composing the resistor array are connected in series and the resistors (R1 to Rn) are connected by short-circuiting wires. Cutting this connection at point a or b, etc. shown in Figure 150 varies the current Ir flowing through the resistor

array 1503. Changes in the current Ir cause changes to the voltage applied to the positive terminal of the operational amplifier 722, resulting in changes in the reference current Ia. The point at which the connection will be cut is determined by monitoring the current flowing through the resistor Rr, in such a way as to produce a target reference current.

To trim the resistor array 1503, laser light 1502 can be emitted from a laser device 1501.

Incidentally it has been stated with reference to Figure 148 that the RGB reference currents are varied by varying the values of RGB resistors 691. Also, it has been stated with reference to Figure 149 that the RGB reference currents are varied by operating the switches Sx in the electronic regulator circuits 561 using values stored in the flash memories 1491. Also, it has been stated with reference to Figure 150 that the RGB reference currents are varied by trimming the resistance values of the resistor array 1503. However, the present invention is not limited to that.

For example, needless to say, the reference currents can be varied by varying the value of each of RGB reference voltages (VrefR, VrefG, and VrefB) in Figures 149 and 150. The RGB reference voltages Vref can be generated easily by an operational amplifier circuit or the like. Also, in Figures 148, 149, 150, etc., by using the resistor Rr as a regulator, it is possible to vary the reference voltage applied to the

source driver circuit (IC) 14, as a result.

It has been stated that 0 to 63 times the current of the final-stage current sources 633 is outputted, but this is true only when the current mirror factor of the final-stage current sources 633 is 1. When the current mirror factor is 2, 0 to 126 times the current of the final-stage current sources 633 is output and when the current mirror factor is 0.5, 0 to 31.5 times the current of the final-stage current sources 633 is output.

Thus, the present invention allows the values of output current to be changed easily by changing the current mirror factor of the final-stage current sources 633 or current sources (631, 632, etc.) in preceding stages. Preferably, the current mirror factor is varied (differed) separately for R, G, and B. The current mirror factor of any current source only for R, for example, may be varied (differed) from the other colors (from the current source circuits for the other colors). EL display panels, in particular, have different luminous efficiencies for different colors (R, G, and B; or cyan, yellow, and magenta). Thus, by varying the current mirror factor among different colors, it is possible to improve the white balance.

The current mirror factor of current sources may be varied (differed) from the other colors (from the current source circuits for the other colors) in an unfixed manner.

It may be variable. The current mirror factor can be made variable by providing a plurality of transistors composing a current mirror circuit in a current source and changing, based on external signals, the number of transistors through which current current is passed. This configuration makes it possible to achieve an optimum white balance through adjustments while observing emission condition of manufactured EL display panels in various colors.

The present invention in particular is configured to connect current sources (current mirror circuits) in multiple stages. Thus, by varying the current mirror factor between the first-stage current source 631 and second-stage current sources 632, it is possible to vary the output currents of a large number of outputs easily using a small number of connections (current mirror circuits and the like). Needless to say, this makes it possible to vary the output currents of a large number of outputs easily using a smaller number of connections (current mirror circuits and the like) than by varying the current mirror factor between the second-stage current sources 632 and third-stage current sources 633.

Incidentally, varying a current mirror factor means varying (adjusting) a magnification factor of current. Thus, it is not limited to current mirror circuits. For example, it can be implemented by an operational amplifier

circuit for current output or a D/A circuit for current output.
The items described above also apply to other examples of the
present invention.

Figure 65 is an exemplary circuit diagram showing 176
outputs (N × M = 176) of a three-stage current mirror circuit.
In Figure 65, the current source 631 constituted of the
first-stage current mirror circuit is referred to as a parent
current source, the current sources 632 constituted of the
second-stage current mirror circuits are referred to as child
current sources, and the current sources 633 constituted of
the third-stage current mirror circuits are referred to as
grandchild current sources. The use of an integral multiple
for the third-stage current mirror circuits which are the
final-stage current mirror circuits makes it possible to
minimize variations in the 176 outputs and produce
high-accuracy current outputs. Of course, it should be
remembered that the current sources 531, 632, and 633 must
be placed densely.

Incidentally, dense placement means placing the first
current source 631 and the second current sources 632 (the
current or voltage output and current or voltage input) at
least within a distance of 8 mm. More preferably, they are
placed within 5 mm. It has been shown analytically that when
placed at this density, the current sources can fit into a
silicon chip with little difference in transistor

characteristics (Vt and mobility (μ)). Similarly, the second current sources 632 and third current sources 633 (the current output and current input) are placed at least within a distance of 8 mm. More preferably, they are placed within 5 mm. Needless to say, the above items also apply to other examples of the present invention.

The current or voltage output and current or voltage input mean the following relationships. In the case of voltage-based delivery shown in Figure 66, the transistor 631 (the output) of the (I)-th current source and the transistor 632a (the input) of the (I + 1)-th current source are placed close to each other. In the case of current-based delivery shown in Figure 67, the transistor 631a (the output) of the (I)-th current source and the transistor 632b (the input) of the (I + 1)-th current source are placed close to each other.

Incidentally, although it is assumed in Figures 65, 66, etc. that there is one transistor 631, this is not restrictive. For example, it is also possible to form a plurality of small sub-transistors 631 and connect the source or drain terminals of the sub-transistors with the variable resistor 651 to form a unit transistor. By connecting the plurality of small sub-transistors in parallel, it is possible to reduce variations of the unit transistor.

Similarly, although it is assumed that there is one transistor 632a, this is not restrictive. For example, it

is also possible to form a plurality of small sub-transistors 632a and connect the gate terminals of the transistors 632a with the gate terminal of the transistor 631. By connecting the plurality of small transistors 632a in parallel, it is possible to reduce variations of the transistor 632a.

Thus, according to the present invention, the following configurations can be illustrated: a configuration in which one transistor 631 is connected with a plurality of transistors 632a, a configuration in which a plurality of transistors 631 are connected with one transistor 632a, and a configuration in which a plurality of transistors 631 are connected with a plurality of transistors 632a. These examples will be described in more detail below.

The above items also apply to a configuration of transistors 633a and 633b in Figure 68. Possible configurations include a configuration in which one transistor 633a is connected with a plurality of transistors 633b, a configuration in which a plurality of transistors 633a are connected with one transistor 633b, and a configuration in which a plurality of transistors 633a are connected with a plurality of transistors 633b. By connecting the plurality of small transistors 633 in parallel, it is possible to reduce variations of the transistor 633.

The above items also apply to relationship between transistors 632a and 632b in Figure 68. Also, preferably a

plurality of transistors 633b are used in Figure 64. Similarly, it is preferable to use plurality of transistors 633 in Figures 73 and 74.

Although description is made as a silicon chip here, this means a semiconductor chip. Thus, the chip as referred to here may be a chip formed on a gallium substrate or other semiconductor chip formed on a germanium substrate or the like. Thus, the source driver IC 14 may be constructed of any semiconductor substrate. Also, the unit transistor 634 may be a bipolar transistor, CMOS transistor, Bi-CMOS transistor, or DMOS transistor. However, in terms of reducing variations in the output of the unit transistor 634, preferably a CMOS transistor is used for the unit transistor 634.

Preferably, the unit transistor 634 is an N-channel transistor. The unit transistor consisting of a P-channel transistor has 1.5 times larger output variations than the unit transistor consisting of an N-channel transistor.

Since it is preferable that the unit transistor 634 of the source driver IC 14 is an N-channel transistor, the programming current of the source driver IC 14 is a current drawn from the pixel 16. Thus, the driver transistor 11a of the pixel 16 is a P-channel transistor. The switching transistor 11d in Figure 1 is also a P-channel transistor.

Thus, the configuration in which the unit transistor 634 in the output stage of the source driver IC (circuit) 14 is

an N-channel transistor and the driver transistor 11a of the pixel 16 is a P-channel transistor is characteristic of the present invention. Incidentally, if all the transistors 11 composing the pixel 16 are illustrated in Figure 1, this is more preferable because this can reduce the number of process masks required to produce the pixel 16.

If P-channel transistors are used as the transistors 11 of pixels 16, programming current flows in the direction from the pixels 16 to the source signal lines 18. Thus, N-channel transistors should be used for the unit transistors 634 (see Figures 73, 74, 126, and 129) of the source driver circuit. That is, the source driver circuit 14 should be configured in such a way as to draw the programming current Iw.

Thus, if the driver transistors 11a of the pixels 16 (in the case of Figure 1) are P-channel transistors, the unit transistors 634 of the source driver circuit 14 must always be N-channel transistors to ensure that the source driver circuit 14 will draw the programming current Iw.
In order to form a source driver circuit 14 on an array board 71, it is necessary to use both masks (processes) for N-channel transistors and masks (processes) for P-channel transistors. Conceptually speaking, in the display panel (display apparatus) of the present invention, P-channel transistors are used for the pixels 16 and gate driver circuits 12 while N-channel transistors are used as the transistors of drawing

current sources of the source drivers.

Thus, P-channel transistors are used as the transistors 11 of pixels 16 and for the gate driver circuits 12. This makes it possible to reduce the costs of the array boards 71. However, in the source driver 14, unit transistors 634 must be N-channel transistors. Thus, the source driver circuit 14 cannot be formed directly on a board 71. Thus, the source driver circuit 14 is made of a silicon chip and the like separately and mounted on the array board 71. In short, the present invention is configured to mount the source driver IC 14 (means of outputting programming current as video signals) externally.

Incidentally, although it has been stated that the source driver circuit 14 is made of a silicon chip, this is not restrictive. For example, a large number of source driver circuits may be formed on a glass substrate simultaneously using low-temperature polysilicon technology or the like, cut off into chips, and mounted on boards 71. Incidentally, although it has been stated that a source driver circuit is mounted on a board 71, this is not restrictive. Any form may be adopted as long as the output terminals 681 of the source driver circuit 14 are connected to the source signal lines 18 of the board 71. For example, the source driver circuit 14 may be connected to the source signal lines 18 using TAB technology. By forming a source driver circuit 14 on a silicon

chip and the like separately, it is possible to reduce variations in output current and achieve proper image display as well as to reduce costs.

The configuration in which P-channel transistors are used as selection transistors of pixels 16 and for gate driver circuits is not limited to organic EL or other self-luminous devices (display panels or display apparatus). For example, it is also applicable to liquid crystal display device and FEDs (field emission displays).

If the switching transistors 11b and 11c of a pixel 16 are P-channel transistors, the pixel 16 becomes selected at Vgh, and becomes deselected at Vgl. As described earlier, when the gate signal line 17a changes from Vgl (on) to Vgh (off), voltage penetrates (penetration voltage). If the driver transistor 11a of the pixel 16 is a P-channel transistor, the penetration voltage more tightly restricts the flow of current through the transistor 11a in black display mode. This makes it possible to achieve a proper black display. The problem with the current-driven system is that it is difficult to achieve a black display.

According to the present invention, because P-channel transistors are used for the gate driver circuits 12, the turn-on voltage corresponds to Vgh. Thus, the gate driver circuits 12 match well with the pixels 16 constructed from P-channel transistors. Also, to improve black display, it

is important that the programming current Iw flows from the anode voltage Vdd to the unit transistors 634 of the source driver circuit 14 via the driver transistors 11a and source signal lines 18, as is the case with the pixel 16 configuration shown in Figures 1, 2, 32, 140, 142, 144, and 145. Thus, a good synergistic effect can be produced if P-channel transistors are used for the gate driver circuits 12 and pixels 16, the source driver circuit 14 is mounted on the substrate, and N-channel transistors are used as the unit transistors 634 of the source driver circuit 14. Besides, unit transistors 634 constituted of N-channel transistors have smaller variations in output current than unit transistors 634 constituted of P-channel transistors. N-channel unit transistors 634 have 1/1.5 to 1/2 as large variations in output current as P-channel unit transistors 634 when they have the same area (W * L). For this reason, it is preferable that N-channel transistors are used as the unit transistors 634 of the source driver IC 14.

The same applies to Figure 42(b). Figure 42(b) shows a configuration in which a programming current Iw flows from an anode voltage Vdd to the unit transistors 634 of a source driver circuit 14 via a programming transistor 11a and source signal line 18 rather than a configuration in which current flows into the unit transistors 634 of a source driver circuit 14 via a driver transistor 11b. Thus, as in the case of Figure

1, a good synergistic effect can be produced if P-channel transistors are used for the gate driver circuits 12 and pixels 16, the source driver circuit 14 is mounted on the substrate, and N-channel transistors are used as the unit transistors 634 of the source driver circuit 14.

According to the present invention, the driver transistors 11a of the pixels 16 are P-channel transistors and the switching transistors 11b and 11c are P-channel transistors. Also, the unit transistors 634 in the output stages of the source driver IC 14 are N-channel transistors. Besides, preferably P-channel transistors are used for the gate driver circuits 12.

Needless to say, a configuration in which P-channel and N-channel transistors are interchanged also works well. Specifically, the driver transistors 11a of the pixels 16 are N-channel transistors and the switching transistors 11b and 11c are N-channel transistors. Also, the unit transistors 634 in the output stages of the source driver IC 14 are P-channel transistors. Besides, preferably N-channel transistors are used for the gate driver circuits 12. This configuration also belongs to the present invention.

The above items apply not only to an IC which contain a single unit transistor 634, but also to a source driver IC 14 with another configuration such as a source driver circuit whose current output stage contains a plurality of transistors

or current mirrors.

Besides, they also apply to source driver circuits 14 by using semiconductor films of low-temperature polysilicon, high-temperature polysilicon, CGS formed by solid-phase growth, or amorphous silicon. In that case, however, panels are often relatively large. On a large panel, it is hard to visually perceive the effect of some variations in the output from the source signal lines 18.

Thus, in the case of a display panel in which a source driver circuit 14 is formed on the glass substrate or the like together with pixel transistors, dense placement means placing the first current source 631 and second current sources 632 (the input and output of current) at least within 30 mm (inclusive) of each other. More preferably, they are within 20 mm (inclusive) of each other. It has been shown analytically that there is little difference in characteristics (Vt and mobility (μ)) of transistors placed in this range. Similarly, the second current sources 632 and third current sources 633 (the input and output of current) are placed at least within 30 mm (inclusive) of each other. More preferably, they are within 20 mm (inclusive) of each other.

It has been stated for ease of understanding and explanation that signals are transferred between current mirror circuits by way of voltage. However, by using current-based delivery. It is possible to reduce variations

in the driver circuit (IC) 14 of a current-driven display panel.

Figure 67 shows an example of configuration for current-based delivery. Figure 66 also shows an example of configuration for current-based delivery. Figures 66 and 67 are similar in terms of circuit diagrams and differ in layout configuration, i.e., wiring layout. In Figure 66, reference numeral 631 denotes an N-channel transistor for the first-stage current source, 632a denotes an N-channel transistor for a second-stage current source, and 632b denotes a P-channel transistor for a second-stage current source.

In Figure 67, reference numeral 631a denotes a first-stage N-channel current source transistor, 632a denotes a second-stage N-channel current source transistor, and 632b denotes a second-stage P-channel current source transistor.

In Figure 66, the gate voltage of the first-stage current source consisting of a variable register 651 (used to vary current) and the N-channel transistor 631 is delivered to the gate of the N-channel transistor 632a of the second-stage current source. Thus, this is a layout configuration of a voltage-based delivery type.

In Figure 67, the gate voltage of the first-stage current source consisting of a variable register 651 and the N-channel transistor 631a is applied to the gate of the N-channel transistor 632a of the adjacent second-stage current source, and consequently the value of the current flowing through the

transistor is delivered to the P-channel transistor 632b of the second-stage current source. Thus, this is a layout configuration of a current-based delivery type.

Incidentally, although this example of the present invention focuses on relationship between the first current source and second current source for ease of explanation or understanding, this is not restrictive and it goes without saying that this example also applies (can be applied) to relationship between the second current source and third current source as well as relationship between other current sources.

In the layout configuration of the current mirror circuit of the voltage-based delivery type shown in Figure 66, the N-channel transistor 631 of the first-stage current source and the N-channel transistor 632a of the second-stage current source composing the current mirror circuit are separated (or liable to get separated, to be precise), and thus the two transistors tend to differ in characteristics. Consequently, the current value of the first-stage current source is not transmitted correctly to the second-stage current source and there can be variations.

In contrast, in the layout configuration of the current mirror circuit of the current-based delivery type shown in Figure 67, the N-channel transistor 631a of the first-stage current source and the N-channel transistor 632a of the

second-stage current source composing the current mirror

circuit are located adjacent to each other (easy to place

adjacent to each other), and thus the two transistors hardly

differ in characteristics. Consequently, the current value

of the first-stage current source is transmitted correctly

to the second-stage current source and there can be little

variations.

In view of the above circumstances, it is preferable to

use a layout configuration of the current-based delivery type

instead of the voltage-based delivery type for the circuit

configuration of the multi-stage current mirror circuit

according to the present invention (the source driver IC

(circuit) 14 of the current-based delivery type according to

the present invention) in terms of reduced variations.

Needless to say the above example can be applied to other

examples of the present invention.

Incidentally, although delivery from the first-stage

current source to the second-stage current source has been

cited for the sake of explanation, the same applies to delivery

from the second-stage current source to the third-stage current

source, delivery from the third-stage current source to the

fourth-stage current source, and so on.

Figure 68 shows a current-based delivery version of

three-stage current mirror circuit (three-stage current

source) shown in Figure 65 (which, therefore shows a circuit configuration of a voltage-based delivery type).

In Figure 68, a reference current is created first by the variable register 651 and N-channel transistor 631. Incidentally, although it is stated that the reference current is adjusted by the variable register 651, actually the source voltage of the transistor 631 is set and regulated by an electronic regulator formed (or placed) in the source driver IC (circuit) 14. Alternatively, the reference current is adjusted by directly supplying the source terminal of the transistor 631 with current outputted from a current-type electronic regulator consisting of a large number of unit transistors (single-unit) 634 as shown in Figure 64 (see Figure 69).

The gate voltage of the first-stage current source constituted of the transistor 631 is applied to the gate of the N-channel transistor 632a of the adjacent second-stage current source, and the current consequently flowing through the transistor is delivered to the P-channel transistor 632b of the second-stage current source. Also, the gate voltage of the P-channel transistor 632b of the second-stage current source is applied to the gate of the N-channel transistor 633a of the adjacent third-stage current source, and the current consequently flowing through the transistor is delivered to the N-channel transistor 633b of the third-stage current source.

A large number of current sources 634 are formed (placed) at the gate of the N-channel transistor 633b of the third-stage current source according to the required bit count as illustrated in Figure 64.

The configuration in Figure 69 is characterized in that the first-stage current source 631 of the multi-stage current mirror circuit is equipped with a current-value adjustment element. This configuration allows output current to be controlled by varying the current value of the first-stage current source 631.

Variations in the Vt of transistors (variations in characteristics) are on the order of 100 mV within a wafer. However, variations in Vt of transistors formed within 100 μ of each other should be 10 mV or less (actual measurement). That is, by configuring a current mirror circuit with transistors formed close to each other, it is possible to reduce variations in the output current of the current mirror circuit. This reduces variations in the output current among terminals of the source driver IC.

Incidentally, although variations in Vt are described as variations among transistors, variations among transistors are not limited to variations in Vt. However, since variations in Vt are a main cause of variations among transistors, it is assumed that the variations in Vt = the variations among transistors, for ease of understanding.

Figure 110 shows formation areas of transistors (square millimeter) versus variations in the output current of unit transistors 484 based on measurement results. The variations in the output current are variations in current at a threshold voltage (Vt). Black dots indicate variations in the output current of evaluation sample transistors (10 to 200 in number) created in a formation area. There is almost no variation (output current variations only within a margin of error, meaning that a constant output current is produced) in the output current of transistors formed in area A (a formation area of 0.5 square millimeters or less) in Figure 110. Conversely, in area C (a formation area of 2.4 square millimeters or more), variations in the output current with respect to the formation area tend to increase sharply. In area B (a formation area of 0.5 to 2.4 square millimeters), variations in the output current are almost proportional to the formation area.

However, the absolute value of output current varies from wafer to wafer. However, this problem can be dealt with by adjusting the reference voltage or setting it to a fixed value in the source driver circuit (IC) 14 of the present invention. Also, it can be dealt with (solved) by modifying the current mirror circuit ingeniously.

The present invention varies (controls) the amount of current flowing through the source signal line 18 by switching

the number of currents flowing through the unit transistors 634 using input digital data (D). When the number of gradations is 64 or more, since 1/64 = 0.015, theoretically variations in output current should be within 1 to 2%. Incidentally, output variations within 1% are difficult to distinguish visually and output variations of 0.5% or below are impossible to distinguish (look uniform).

To keep output current variations (%) within 1%, the formation area of a transistor group (the transistors among which variations should be suppressed) should be kept within 2 square millimeters as indicated by the results shown in Figure 110. More preferably, the output current variations (i.e., variations in the Vt of transistors) should be kept within 0.5%. That is, the formation area of a transistor group 681 can be kept within 1.2 square millimeters as indicated by the results shown in Figure 110. Incidentally, the formation area is given by the vertical length multiplied by the horizontal length. For example, a formation area of 1.2 square millimeters results from 1 mm × 1.2 mm.

Incidentally, the above applies to 8-bit (256 gradations) or larger data. For a smaller number of gradations, for example, in the case of 6-bit data (64 gradations), variations in output current may be somewhere around 2% (virtually no problem in terms of image display). In this case, the formation area of a transistor group 681 can be kept within 5 square millimeters.

There is no need for the two transistor groups 681 (transistor groups 681a and 681b are shown in Figure 68) to satisfy this condition. Effect of the present invention can be achieved if at least one of the transistor groups (one or more transistor groups 681 if there are more than three) satisfy the condition. Preferably, this condition should be satisfied for a lower level transistor group 681 (681a is higher than 681b). This will reduce image display problems.

In the source driver circuit (IC) 14 of the present invention, at least a plurality of current sources, such as consisting of parent, child, and grandchild current sources, are connected in multiple stages (of course there may be two stages consisting of parent and child current sources) and placed densely, as shown in Figure 68. Current-based delivery is made between current sources (between the transistor groups 681). Specifically, transistors enclosed by dotted lines in Figure 68 (transistor groups 681) are placed densely. The transistor groups 681 make voltage-based delivery between each other. The parent current source 631 and child current sources 632a are formed (placed) approximately in the center of the source driver IC chip 14. This makes it possible to relatively shorten the distance between the transistors 632a composing the child current sources placed on the left and right of the chip and the transistors 632b composing current child sources. That is, the top-level transistor group 681a is placed at the

approximate center of the IC chip. Then, lower-level transistor groups 681b are placed on the left and right of the IC chip 14. Preferably, the transistors are placed, formed, or produced in such a way that approximately equal numbers of lower-level transistor groups 681b will be on the left and right of the IC chip 14. Incidentally, the above items are not limited to IC chips 14, but apply to source driver circuits 14 formed directly on array boards 71 using low-temperature polysilicon technology or high-temperature polysilicon technology. The same is true of the other items.

According to the present invention, one transistor group 681a is constructed, placed, formed, or built at the approximate center of the IC chip 14 and eight transistor groups 681b each are formed on the left and right of the chip (N = 8 + 8, see Figure 63). Preferably the child transistor groups 681b are arranged in such a way that their numbers will be equal on the left and right of the chip or that the difference between the number of the child transistor groups 681b formed or placed on the left with respect to the center of the chip where the parent is formed and the number of the child transistor groups 681b formed or placed on the right of the chip will be four or less. More preferably, the difference between the number of the child transistor groups 681b formed or placed on the left of the chip and the number of the child transistor groups 681b formed or placed on the right of the chip is one

or less. The above items similarly apply to grandchild transistor groups (omitted in Figure 68).

Voltage-based delivery (voltage connection) is made between the parent current source 631 and child current sources 632a. Consequently, tends to be affected by variations in the Vt of the transistors. Thus, the transistors in the transistor group 681a are placed densely. The formation area of the transistor group 681a is kept within 2 square millimeters as shown in Figure 110. More preferably, it is kept within 1.2 square millimeters. If the number of gradations is 64 or less, of course, the formation area may be within 5 square millimeters.

Data is delivered between the transistor group 681a and child transistors 632b via current, and thus the current may flow some distance. Regarding the distance (e.g., between the output terminals of the higher-level transistor group 681a and input terminals of the lower-level transistor group 681b), the transistors 632a composing the second current sources (child) and the transistors 632b composing the second current sources (child) should be placed at least within 10 mm of each other as described above. Preferably, the transistors should be placed or formed within 8 mm. More preferably, they should be placed within 5 mm.

It has been shown analytically that differences in characteristics (Vt and mobility (μ)) of transistors placed

in a silicon chip do not have much impact in the case of current-based delivery if the distance is within this range. Preferably, the above conditions are satisfied especially by lower-level transistor groups. For example, if the transistor group 681a is at the top level with the transistor groups 681b lying below it and transistor groups 681c lying further below them, the current-based delivery between the transistor groups 681b and transistor groups 681c should satisfy the above conditions. Thus, according to the present invention it is not always necessary that all the transistor groups 681 satisfy the above conditions. It is sufficient that at least a pair of transistor groups 681 satisfy the above conditions. This is because the lower the level, the more transistor groups 681 there are.

This similarly applies to the transistors 633a constituting the third (grandchild) current sources and transistors 633b constituting the third current sources. Needless to say, almost the same applies to voltage-based delivery. The transistor groups 681b are formed, built, or placed in the left-to-right direction of the chip (in the longitudinal direction, i.e., at locations facing the output terminal 761). The transistor groups 681b are formed, built, or placed in the left-to-right direction of the chip (in the longitudinal direction, i.e., at locations facing the output

terminal 761). According to the present invention, the number
M of the transistor groups 681b is 11 (see Figure 63).

Voltage-based delivery (voltage connection) is made
between the child current sources 632b and grandchild current
sources 633a. Thus, the transistors in the transistor groups
681b are placed densely as is the case with the transistor
group 681a. The formation area of the transistor group 681b
should be within 2 square millimeters as shown in Figure 110.
More preferably, it should be within 1.2 square millimeters.
However, even slight variations in the Vt of the transistors
in the transistor groups 681b tend to appear on the screen.
Thus, preferably the formation area should be area A (0.5 square
millimeters or less) in Figure 110.

Data is delivered between the grandchild transistors 633a
and transistors 633b (current-based delivery), and thus the
current may flow some distance in the transistor group 681b.
The description of distances provided earlier applies here
as well. The transistors 633a constituting the third
(grandchild) current sources and transistors 633b
constituting the second (grandchild) current sources should
be placed within at least 8 mm of each other. More preferably,
they should be placed within 5 mm.

Figure 69 shows the current-value adjustment element
constituted of an electronic regulator. The electronic
regulator consists of a resister 691 (which is formed of

polysilicon, controls current, and creates reference voltages), decoder circuit 692, level-shifter circuit 693, etc. Incidentally, the electronic regulator outputs current. A transistor 641 functions as an analog switch circuit.

Incidentally, in the source driver IC (circuit) 14, transistors may be referred to as current sources. This is because transistors function as current sources in current mirror circuits and the like composed of transistors.

Electronic regulators circuits are formed (or placed) according to the number of colors used by the EL display panel. For example, if the three primary colors RGB are used, preferably three electronic regulators are formed (or placed) corresponding to the colors so that the colors can be adjusted independently. However, if one color is used as a reference (is fixed), as many electronic regulators circuits as the number of colors minus 1 should be formed (or placed).

Figure 76 shows a configuration in which resistive elements 651 are formed (or placed) to control reference voltages of the three primary colors RGB independently. Of course, it goes without saying that the resistive elements 651 may be substituted with electronic regulators. Basic current sources including parent and child current sources such as the current source 631 and current sources 632 are placed densely in an output current circuit 704 in an area illustrated in Figure 76. The dense placement reduces

variations in outputs from the source signal lines 18. As illustrated in Figure 76, by placing them in the output current circuit 704 at the center of the source driver IC (circuit) 14, it becomes easy to distribute current to the left and right of the source driver IC (circuit) 14 from the current source 631 and current sources 632, resulting in reduced output variations between the left and right sides (it is all right to place them in a reference current generator circuit or controller instead of the current output circuit. That is, 704 is an area where an output circuit is not formed).

However, it is not always necessary to place them in the output current circuit 704 at the center They may be placed at an end or both ends of the IC chip. Also, they may be formed or placed in parallel with the output current circuit 704.

It is not desirable to form a controller or output current circuit 704 in the center of the IC chip 14 because they are liable to be affected by Vt distribution of the unit transistors 634 in the IC chip 14 (the Vt of an wafer is distributed evenly in the wafer).

Reasons for this will be described with reference to Figure 120. If the controller or output current circuit 704 is formed in the center of the IC chip 14, it is not possible to form or construct an output current circuit constituted of unit transistors 634 in the center. On the other hand, pixels 16 are formed in a matrix in the display screen 50 of the display

panel. The pixels are formed in a grid pattern at equal intervals. Consequently, as illustrated in Figure 120, there is no output terminal 761b of the output current circuit in the center of the IC chip 14. Thus, wires are routed to the center portion of the display screen 50 of the display panel from output terminals 761a and 761c other than those in the center of the EL element 15.

However, there is a possibility that the unit transistors of the output circuits connected to the output terminals 761b and 761c differ in Vt. Even if the unit transistors 634 of the output terminals have equal gate terminal voltage, their output current will vary depending on the Vt distribution of the unit transistors 634. Consequently, there may be steps of output currents in the center of the panel. The steps of output currents can cause brightness difference between the right and left sides in the center of the screen.

A configuration used to solve this problem is shown in Figure 122. Figure 122(a) shows an exemplary configuration in which an output current circuit 704 is placed on one side of an IC chip. Figure 122(b) shows an exemplary configuration in which output current circuits 704 are placed on both sides of an IC chip. Figure 122(c) shows an exemplary configuration in which an output current circuit 704 is placed on the side of input terminals of an IC chip. Thus, output terminals are formed orderly in areas not occupied by the output current

circuits 704.

In the circuit configuration in Figure 68, transistors 633a and transistors 633b are connected in a one-to-one completion. In Figure 67 again, transistors 632a and transistors 632b are connected in a one-to-one completion.

However, if transistors are connected in a one-to-one relationship with other transistors, any variation in the characteristics (Vt, etc.) of characteristics of a transistor will result in variations in the output of the corresponding transistor connected to it.

To solve this problem, an example with an appropriate configuration is shown in Figure 123. In the configuration shown in Figure 123, transmission transistor groups 681b (681b1, 681b2, and 681b3) each of which consists of four transistors 633a and transmission transistor groups 681c (681c1, 681c2, and 681c3) each of which consists of four transistors 633b are connected with each other. Although it has been stated that each of the transistor groups 681b and 681c consist of four transistors 633, this is not restrictive and may consist of less than four or more than four transistors. That is, a reference current Ib flowing through the transistors 633a is output from a plurality of transistors 633 which form a current mirror circuit together with the transistors 633a and the output current is received by a plurality of transistors 633b.

Preferably, the plurality of transistors 633a and plurality of transistors 633b are approximately equal in size and equal in number. Preferably, the unit transistors 634 (63 in number in the case of 64 gradations as in Figure 124) each of which produces one output and the transistors 633b which compose a current mirror together with the unit transistors 634 are also approximately equal in size and equal in number. The above configuration makes it possible to set a current mirror ratio accurately and reduce variations in output current.

Preferably, the current flowing through the transistors 633b is equal to or more than five times a current Ic1 passed through the transistors 632b. This will stabilize the gate potential of the transistors 633a and suppress transient phenomena caused by output current.

Although it has been stated that the transmission transistor group 681b1 and transmission transistor group 681b2 are placed adjacent to each other and that each of them consists of four transistors 633a placed next to one another, this is not restrictive. For example, the transistors 633a of the transmission transistor group 681b1 and the transistors 633a of the transmission transistor group 681b2 may be placed or formed alternately. This will reduce variations in the output current (programming current) of each terminal.

The use of multiple transistors for current-based delivery makes it possible to reduce variations in output current of the transistor group as a whole and further reduce variations in the output current (programming current) of each terminal.

The total formation area of the transistors 633 composing a transmission transistor group 681 is an important item. Basically, the larger the total formation area of the transistors 633, the smaller the variations in output current (programming current flowing in from the source signal line 18). That is, the larger the formation area of the transmission transistor group 681 (the total formation area of the transistors 633), the smaller the variations. However, a larger formation area of the transistors 633 increases a chip area, increasing the price of the IC chip 14.

Incidentally, the formation area of a transmission transistor group 681 is the sum total of the formation areas of the transistors 633 composing the transmission transistor group 681. The area of a transistor 633 is the product of the channel length L and channel width W of the transistor 633. Thus, if a transistor group 681 consists of ten transistors 633 whose channel length L is 10 μm and channel width W is 5 μm, the formation area Tm (square μm) of the transmission transistor group 681 is 10 μm × 5 μm × 10 = 500 (square μm).

The formation area of the transmission transistor group 681 should be determined in such a way as to maintain a certain relationship with the unit transistors 634. Also, the transmission transistor group 681a and transmission transistor group 681b should maintain a certain relationship.

Now, description will be given of the relationship between the formation area of the transistor group 681 and the unit transistors 634. As also illustrated in Figure 66, a plurality of unit transistors 634 are connected per one transistor 633b. In the case of 64 gradations, 63 unit transistors 634 correspond to one transistor 633b (configuration in Figure 64). If the channel length L of the unit transistor 633 is 10 μm and channel width W of the unit transistor 633 is 10 μm, the formation area Ts (square μm) of the unit transistor group is 10 μm × 10 μm × 63 = 6300 square μm.

The transistor 633b in Figure 64 and transmission transistor groups 681c in Figure 123 are relevant here. The formation area Ts of the unit transistor group and formation area Tm of the transmission transistor group 681c have the following relationship:

$1/4 \leq Tm/Ts \leq 6$

More preferably, the formation area Ts of the unit transistor group and formation area Tm of the transmission transistor group 681c have the following relationship:

$1/2 \leq Tm/Ts \leq 4$

By satisfying the above relationship, it is possible to reduce variations in the output current (programming current) of each terminal.

Also, the formation area Tmm of the transmission transistor group 681b and formation area Tms of the transmission transistor group 681c have the following relationship:

$1/2 \leq Tmm/Tms \leq 8$

More preferably, the formation area Ts of the unit transistor group and formation area Tm of the transmission transistor group 681c have the following relationship:

$1 \leq Tm/Ts \leq 4$

By satisfying the above relationship, it is possible to reduce variations in the output current (programming current) of each terminal.

Suppose output current from the transistor group 681b1 is Ic1, output current from the transistor group 681b2 is Ic2, and output current from the transistor group 681b2 is Ic3. Then, the output currents Ic1, Ic2, and Ic3 must coincide. According to the present invention, since each transistor group 681 consists of multiple transistors 633, even if individual transistors 633 have variations, there is no variation in the output current Ic of the transistor group 681 as a whole.

Incidentally, the above example is not limited to three-stage current mirror connections (multi-stage current

mirror connections) shown in Figure 68. Needless to say, it is also applicable to single-stage current mirror connections. The example shown in Figure 123 involves connecting the transistor groups 681b (681b1, 681b2, 681b3, ...) each of which consists of multiple transistors 633a with the transistor groups 681c (681c1, 681c2, 681c3, ...) each of which consists of multiple transistors 633b. However, the present invention is not limited to this. It is also possible to connect a single transistor 633a with the transistor groups 681c (681c1, 681c2, 681c3, ...) each of which consists of multiple transistors 633b, or to connect the transistor groups 681b (681b1, 681b2, 681b3, ...) each of which consists of multiple transistors 633a with one transistor group 633b.

In Figure 64, the switch 641a corresponds to the 0th bit, the switch 641b corresponds to the 1st bit, the switch 641c corresponds to the 2nd bit, ..., and the switch 641f corresponds to the 5th bit. The 0th bit consists of one unit transistor, the 1st bit consists of two unit transistor, the 2nd bit consists of four unit transistor, ..., and the 5th bit consists of thirty-two (32) unit transistor. For ease of explanation, it is assumed that the source driver circuit 14 is a 6-bit driver supporting 64-gradation display.

With the configuration of the driver 14 according to the present invention, the 1st bit outputs a twice larger programming current to the 0th bit, the 2nd bit outputs a twice

larger programming current to the 1st bit, the 3rd bit outputs a twice larger programming current to the 2nd bit, the 4th bit outputs a twice larger programming current to the 3rd bit, the 5th bit outputs a twice larger programming current to the 4th bit. To put it in other words, each bit must be able to output twice as large programming current as the next lower-order bit.

However, in practice because of variations in the unit transistors 634 constituting different bits, it is difficult (if not impossible) to configure such that each terminal will output exactly twice larger programming current.
An example which can solve this problem is shown in Figure 124.

The configuration in Figure 124 contains adjustment transistors in addition to the unit transistors 634 for individual bits.
The adjustment transistors 1241 correspond to the 5th bit (switch 641f) and 4th bit (switch 641e).

In the example shown in Figure 124, the adjustment transistors 1241 are placed, formed, or constructed at the 5th bit (the unit transistors 634 connected to the switch 641f) and 4th bit (the unit transistors 634 connected to the switch 641d). Four adjustment transistors 1241 each are placed or formed at the 5th bit and 4th bit. However, the present invention is not limited to this. The number of adjustment

transistors 1241 for each bit may be changed. Also, adjustment transistors 1241 may be attached to all the bits (by forming, constructing, or placing them). The adjustment transistors 1241 are made smaller than the unit transistors 634. Alternatively, they are designed to produce smaller output current than the unit transistors 634. Even if transistor size is fixed, it is possible to vary output current by varying W/L.

Incidentally, the adjustment transistors 1241 and unit transistors 634 are configured or connected so as to share gate terminals, to which the same gate voltage is applied. Thus, when a current Ib flows through the transistors 633, the gate voltage of the unit transistors 634 is established, prescribing the current to be output from the unit transistors 634. At the same time, output current of the adjustment transistors 1241 is also defined. That is, the output current of the adjustment transistors 1241 is proportional to the output current of the unit transistors 634. The output current can be controlled by means of the current Ib to be passed to the transistors 633 which pair up with the unit transistors 634.

According to the present invention, the size of one unit transistor 634 is made larger than the total size of two or more adjustment transistors. That is, the size of the unit transistor 634 is larger than the size of the adjustment

transistor 1241. Alternatively, the total size of two or more adjustment transistors 1241 is made larger than the size of the unit transistor 634. By controlling the number of working adjustment transistors 1241, it is possible to adjust variations in output current for each bit in small increments.

According to another example of the present invention, the output current of one unit transistor 634 is made larger than the output current of two or more adjustment transistors. That is, the output current of the unit transistor 634 is larger than the output current of the adjustment transistor 1241. By controlling the number of working adjustment transistors 1241, it is possible to adjust variations in output current for each bit in small increments.

Figure 125 is an explanatory diagram illustrating a method of adjusting the output current for each bit using the adjustment transistors 1241.

Figure 125 shows four adjustment transistors 1241 which have been formed. Incidentally, it is assumed for ease of explanation that a target output current of the bit for output current adjustment is Ia and that actual output current Ib is smaller than the target output current Ia by Ie (Ia = Ib + Ie). Also, if Ig is current which flows when all the four adjustment transistors 1241 operate normally, Ig > Ie should always be satisfied even if there are variations in production processes of transistors. Thus, when the four adjustment

transistors 1241 are in operation, the output current Ib exceeds the target output current Ia (Ib >Ia).

In the above condition, adjustment transistors 1241 are cut off from the common terminal 1252 to obtain the target output current Ia. Laser cutting is used to cut off the adjustment transistors 1241. It is appropriate to use a YAG laser for the laser cutting. Besides, neon helium lasers and carbon dioxide lasers are also available. Also, machining such as sand blasting is available as well.

In Figure 125, the transistors 1241a and 1241b are cut off from the common terminal 1252 at two cutting sites 1251. Consequently, the current Ig is halved. In this way, adjustment transistors 1241 are cut off one by one from the common terminal 1252 until the target output current Ia is obtained. The output current is measured with a microammeter to stop cutting off adjustment transistors 1241 when the measured value reaches the target value.

Incidentally, although it has been stated with reference to Figure 125 that the cutting sites 1251 are cut with laser to adjust the output current, this is not restrictive. For example, laser may be emitted directly to adjustment transistors 1241 to adjust the output current by destroying them. It is also possible to provide analog switches at the cutting sites 1251, turn on and off the analog switches by external control signals, and thereby vary the number of

adjustment transistors 1241 to be connected to point g.
That is, the present invention forms adjustment transistors
1241 and obtains target output current by turning on and off
the adjustment transistors 1241. Thus, needless to say, other
configurations can also be used.

Also, it is not strictly necessary to perform cutting
at the cutting sites 1251, and it is alternatively possible
to open the cutting sites in advance and make connections by
depositing a metal film or the like on the cutting sites.

Besides, although it has been stated that the adjustment
transistors 1241 are formed in advance, this is not restrictive.
For example, it is also possible to trim part of the unit
transistors 634, and thereby adjust the output current of the
unit transistors 634 so as to obtain the target output current
for each bit. Alternatively, it is possible to obtain the
target output currents for different bits by separately
adjusting the gate terminal voltages of the unit transistors
634 which correspond to the respective bits. For example,
this can be accomplished by trimming the wiring connected to
the gate terminals of the unit transistors 634 and thereby
increasing resistance.

Figure 166 illustrates part of the adjustment transistors
1241 or unit transistors 634. A plurality of unit transistors
634 (or the adjustment transistors 1241) are connected via
internal wiring 1622. The adjustment transistors 1241 have

a slit cut in their source terminals (S terminals) for ease of trimming. By making a cut at a cutoff point 1661b, it is possible to limit the current flowing between channels of the adjustment transistors 1241. This decreases output current in a current output stage 704. Incidentally, a slit may be formed not only in the source terminal, but also in the drain or gate terminal. Needless to say, part of the adjustment transistors 1241 can be cut off even if no slit is formed. It is also possible to form a plurality of adjustment transistors 1241 of different shapes, trim the adjustment transistors 1241 after measurement of output current, and thereby select the transistors which will produce output current closest to the target output current.

Incidentally, although unit transistors 634 or adjustment transistors 1241 are trimmed to adjust output current in the above example, the present invention is not limited to this. For example, it is possible to form adjustment transistors 1241 in isolation, connect their source terminals or the like to output current circuits 704 by a FIB process, and thereby adjust output current. However, there is no need to isolate the adjustment transistors 1241 completely. For example, it is possible to form output current circuits 704 and adjustment transistors 1241 with their gate terminals and source terminals connected and connect the drain terminals of the adjustment transistors 1241 by a FIB process.

Also, it is possible to construct the gate terminals of adjustment transistors 1241 in isolation from the gate terminals of unit transistors 634, which form the output current circuits 704, and form or place the unit transistors 634 and the adjustment transistors 1241 with their drain terminals and source terminals connected. The potential at the gate terminals of the unit transistors 634 is determined by current Ic as illustrated in Figure 164 and the like. The potential at the gate terminals of the adjustment transistors 1241 can be adjusted freely. By adjusting this potential, it is possible to change the output current of the adjustment transistors 1241. Thus, by adjusting the potential at the gate terminals of the adjustment transistors 1241, it is possible to adjust the output current of the output current circuits 704, which is a sum total of the output currents from the unit transistors 634 and adjustment transistors 1241. This method does not require a trimming process or FIB process. The gate terminal voltage of the adjustment transistors 1241 may be adjusted using an electronic regulator or the like.

Although it has been stated that the output current of the adjustment transistors 1241 is adjusted through adjustment of the potential at the gate terminals, this is not restrictive. The output current may be adjusted through adjustment of the voltage applied to the source terminals or drain terminals of the adjustment transistors 1241. These terminal voltages

may also be adjusted using an electronic regulator. Also the voltages applied to the terminals of the adjustment transistors 1241 are not limited to direct-current voltages. It is also possible to apply rectangular voltages (pulsed voltages or the like) and control output voltages by duration control.

To change the magnitude of output current greatly, the adjustment transistors 1241 may be cut off at a cutoff point 1661a as illustrated in Figure 166. In this way, by trimming all or part of the unit transistors 634 or adjustment transistors 1241, it is possible to adjust the output current easily. To protect trimming sites from degradation, it is recommended to seal them by vapor-depositing or applying inorganic or organic material to them after trimming so that they will not be exposed to the air.

In particular, preferably the output current circuits 704 on both ends of the IC chip 14 are equipped with a trimming function. In the case of a large display panel, a plurality of source driver ICs 14 must be cascaded. This is because cascade connection makes any difference between output currents of adjacent ICs conspicuous as a boundary. By trimming transistors and the like as illustrated in Figure 166, it is possible to correct output current variations among adjacent output current circuits.

Needless to say, the above is also applicable to other examples of the present invention.

The configuration in Figure 123 reduces variations in the output current of each terminal by making a plurality of transistors 633b receive output current from a plurality of transistors 633a. Figure 126 shows a configuration which reduces variations in the output current of each terminal by supplying current from both sides of a transistor group. Multiple sources are provided for current Ia. Current Ia1 and current Ia2 have the same current value and the transistor which generates the current Ia1 and the transistor which generates the current Ia2 compose a current mirror circuit as a pair.

Thus, in this configuration, a plurality of transistors (current generating means) are formed, placed, or constructed to generate reference currents which prescribe output currents of the unit transistors 634. More preferably, output currents from the plurality of transistors are connected to current-receiving circuits such as transistors which compose current mirror circuits and the output currents of the unit transistors 634 are controlled by gate voltages generated by the plurality of transistors.

Further, an embodiment according to Figure 126 shows transistors 633b composing current mirror circuits are formed on both sides of the group of the unit transistors 634. However, the present invention is not limited to this. A configuration in which transistors 632a composing current

mirrors are placed on both sides of a transistor group 681b
also belongs to the present invention.

As can be seen from Figure 126, the transistor group 681b
contains a plurality of transistors 633a which output current.
On both sides of the transistor group 681b, there are
transistors 632a (632a1 and 632a2) which share the gate
terminals of the transistor group 681b and form current mirrors
circuit in conjunction with transistors 633a.
A reference current Ia1 flows through the transistor 632a1
and a reference current Ia2 flows through the transistor 632a2.
Thus, the gate terminal voltage of the transistors 633a (633a1,
633a2, 633a3, 633a4, ...) are defined by the transistors 632a1
and 632a2, and define the current outputted from the
transistors 633a.

The magnitudes of the reference currents Ia1 and Ia2 are
made to coincide. This can be accomplished by
constant-current circuits such as the current mirror circuit
which output the reference currents Ia1 and Ia2.
Even if the reference currents Ia1 and Ia2 deviate more or
less from each other, this poses little problem because they
correct each other.

Although it has been stated in the above example that
the reference currents Ia1 and Ia2 are made to roughly coincide,
the present invention is not limited to this. For example,
the reference currents Ia1 and Ia2 may be different from each

other. For example, if the current Ia1 is smaller than the current Ia2, a current Ib1 outputted by a transistor 633a1 can be made smaller than a current Ibn outputted by a transistor 633an (Ib1 < Ibn). The smaller the current Ib1, the smaller the current outputted by a transistor group 681c1. The larger the current Ibn, the larger the current outputted by a transistor group 681cn. The transistor groups 681 placed or formed between the transistor group 681c1 and transistor group 681cn produce output currents of intermediate magnitudes.

Thus, by making the current Ia1 and current Ia2 different from each other, it is possible to produce a slope in the output currents of the transistor groups 681. The sloping of the output currents of the transistor groups 681 is effective for cascade connection of the source driver ICs 14. This is because adjustments of the two reference currents Ia1 and Ia2 for IC chips make it possible to adjust the output currents of the output current circuits 704. Thus, it is possible to make adjustments so as to eliminate differences between output currents of adjacent ICs chip 14.

Even if the current Ia1 and current Ia2 are made different from each other, if the potentials at the gate terminals of the unit transistors 634 in the transistor groups 681 are equal, it is not possible to produce a slope in the output currents of the transistor groups 681. The reason why a slope is produced in the output currents of the transistor groups 681

is that the gate terminal voltage differs among the unit transistors 634. To vary the gate terminal voltage, it is necessary to increase the resistance of gate wiring 1261 in the transistor group 681b. Specifically, the gate wiring 1261 is formed of polysilicon. Also, the resistance value of the gate wiring between the transistors 632a1 and 632an should be between 2 KΩ and 2 MΩ (both inclusive). In this way, by increasing the resistance of the gate wiring 1261, it is possible to produce a slope in the output currents of the transistor groups 681c.

Preferably, the gate terminal voltage of the transistor 633a is set at 0.52 to 0.68 V (both inclusive) is a silicon IC chip is used. This range can reduce variations in the output current of the transistor 633a. The above items similarly apply to other examples of the present invention.

Needless to say, the above items also apply to other examples of the present invention.

In the configuration shown in Figure 126, the current mirror circuit contains two or more (multiple) transistors 632a which pair with the transistors 633a. Since reference current are supplied from both sides, the gate terminal voltage of the transistors 633a is kept constant reliably in the transistor group 681a. Consequently, variations in the output current produced by the transistors 633a are extremely small. Thus, there are extremely small variations in the

programming current outputted to the source signal line 18 or programming current drawn from the source signal line 18.

In Figure 126, current is transferred between the transistor 633a1 and transistor 633b1 as well as between the transistor 633a2 and transistor 633b2. Thus, the transistor group 681c1 is also configured to be supplied with current from both sides. Similarly, current is transferred between the transistor 633a3 and transistor 633b3 as well as between the transistor 633a4 and transistor 633b4. Also, current is transferred between the transistor 633a5 and transistor 633b5 as well as between the transistor 633a6 and transistor 633b6.

The transistor groups 681c constitute output-stage circuits connected to respective source signal lines 18. Thus, by supplying current to the transistor groups 681c from both sides and eliminating voltage drops or potential distribution of the gate terminals of the unit transistors 634, it is possible to do away with variations in output currents from the source signal lines 18.

Each transistor group 681c contains a plurality of unit transistors 634 which output current. On both sides of the transistor group 681c, there are transistors 633b (633b1 and 633b2) which share the gate terminals of the transistors 634 and form current mirror circuits in conjunction with the transistors 634. The reference current Ib1 flows through the transistor 633b1 and the reference current Ib2 flows through

the transistor 633b2. Thus, the gate terminal voltage of the unit transistors 634 are defined by the transistors 633b1 and 633b2, and define the current outputted from the unit transistors 634.

The magnitudes of the reference currents Ib1 and Ib2 are made to coincide. This can be accomplished by constant-current circuits such as the transistors 633a which output the reference currents Ib1 and Ib2. Even if the reference currents Ib1 and Ib2 deviate more or less from each other, this poses little problem because they correct each other.

Figure 127 shows a variation of the example shown in Figure 126. In Figure 127, there is a transistor 632 which forms a current mirror circuit in the middle of the transistor group 681b in addition to the transistors 632a which form current mirror circuits on both sides of the transistor group 681b. Consequently, the transistors 633a have a more constant gate terminal voltage and less variations in its output, compared with the configuration shown in Figure 126.
Needless to say, the above items are also applicable to the transistor groups 681c.

Figure 128 shows another variation of the example shown in Figure 126. In Figure 126, the transistors 633a in the transistor group 681b are connected in sequence with the transistors 633b which form current mirror circuits ·in

conjunction with the transistor groups 681c.

In the example shown in Figure 128, the transistors 633a are connected in a different order.

In Figure 128, the transistor 633a1 performs current-based delivery to/from the transistor 633b1 which form a current mirror circuit in conjunction with the transistor group 681c1. The transistor 633a2 performs current-based delivery to/from the transistor 633b3 which form a current mirror circuit in conjunction with the transistor group 681c2. The transistor 633a3 performs current-based delivery to/from the transistor 633b2 which form a current mirror circuit in conjunction with the transistor group 681c1. The transistor 633a4 performs current-based delivery to/from the transistor 633b5 which form a current mirror circuit in conjunction with the transistor group 681c3. The transistor 633a5 performs current-based delivery to/from the transistor 633b4 which form a current mirror circuit in conjunction with the transistor group 681c2.

With the configuration shown in Figure 126, any characteristic distribution of the transistors 633a tends to cause the transistor groups 681c supplied with current from the transistors 633a to form blocks, resulting in changes in output current. Consequently, block-shaped boundaries may appear on the EL display panel.

As shown in Figure 128, by rearranging the order of

connection with the transistors 633 which form current mirror circuits in conjunction with the transistor groups 681c instead of connecting the transistors 633a in order, it is possible to reduce changes in output current caused by blocks formed by the transistor groups 681c even if there is characteristic distribution of the transistors 633a. This prevents block-shaped boundaries from appearing on the EL display panel.

Of course, the transistors 633a and transistors 633b need not be connected regularly, and may be connected randomly. Besides, the transistors 633a may be connected with the transistors 633b by skipping two or more instead of skipping one as shown in Figure 128.

In the above example, current mirror circuits are connected in multiple stages as illustrated in Figure 68. However, the present invention is not limited to multi-stage circuit configurations and can employ single-stage circuit configurations as illustrated in Figure 129.

Figure 129 controls or adjusts a reference current by a reference current regulating means 651 (which, needless to say, is not limited to a variable regulator, and may be an electronic regulator). The unit transistors 634 form current mirror circuits in conjunction with the transistors 633b. The reference current Ib defines the magnitude of output current from the unit transistors 634.

With the configuration shown in Figure 129, the reference

current Ib controls the currents of the unit transistors 634 in the transistor groups 681c. To put it in other words, the transistors 633b define the programming current for the unit transistors 634 in the transistor groups 681c1 to 681cn.

However, there are often subtle differences between the gate terminal voltage of the unit transistors 634 in the transistor group 681c1 and the gate terminal voltage of the unit transistors 634 in the transistor group. This is presumed to be due to voltage drops and the like caused by current flowing through the gate wiring and the like. Even a subtle change in voltage will result in a few percent change in output current (programming current). According to the present invention, difference among gradations is 1.5% (= 100/64) in the case of 64 gradations. Thus, changes in output current should be reduced to at least on the order of 1% or less.

A configuration used to solve this problem is shown in Figure 130. In Figure 130, there are two generator circuits of the reference current Ib. A reference current generator circuit 1 delivers reference current Ib1 and a reference current generator circuit 2 delivers reference current Ib2. The reference current Ib1 and reference current Ib2 have the same current value. The reference currents are controlled or adjusted by a reference current regulating means 651 (which, needless to say, is not limited to a variable regulator, and may be an electronic regulator. Alternatively, the reference

currents may be adjusted by changing fixed resistors).
Incidentally, the output terminals of the transistor groups
681c are connected to the source signal lines 18. The
configuration used here is a single-stage current mirror
circuit.

However, if the reference current Ib1 and reference
current Ib2 are configured to be separately adjustable, it
is possible to adjust output current (programming current)
to be uniform when voltage at point a and voltage at point
b on a common terminal 1253 differ from each other and the
unit transistors 634 in the transistor group 681c1 and unit
transistors 634 in the transistor group 681c2 differ in output
current. Also, since unit transistors on left and right sides
of the IC chip 14 differ in Vt, it is possible to eliminate
a slope in output current and correct any slope which is
produced.

Although two reference current generator circuits are
formed separately in Figure 130, this is not restrictive and
they may be constructed of the transistors 633a in the
transistor group 681b shown in Figure 128. By using the
configuration in Figure 128 and controlling (adjusting) the
current passed through the transistors 632a composing current
mirrors, it is possible to simultaneously control (adjust)
the reference currents Ib1 and Ib2 shown in Figure 130.
That is, the transistors 633b1 and 633b2 are controlled as

a transistor group (see Figure 130(b)).

The use of the configuration in Figure 130 makes it possible to equalize the voltage at point a and voltage at point b on the common terminal 1253 (gate wiring 1261). This makes it possible to equalize the output current of the unit transistors 634 in the transistor group 681c1 and the output current of the unit transistors 634 in the transistor group 681c2 and supply uniform programming current free of variations to the source signal lines 18.

In this way, the configuration in Figure 130 contains two reference current sources. Figure 131 shows a configuration in which gate voltage of a transistor 633b constituting a reference current source is applied to the center of the common terminal 1253 as well.

The reference current generator circuit 1 delivers the reference current Ib1 and the reference current generator circuit 2 delivers the reference current Ib2.
A reference current generator circuit 3 delivers reference current Ib3. The reference current Ib1, reference current Ib2, and reference current Ib3 have the same current value. The reference currents are controlled or adjusted by a reference current regulating means 651 (which, needless to say, is not limited to a variable regulator, and may be an electronic regulator).

If the reference current Ib1, reference current Ib2, and

reference current Ib3 are configured to be separately
adjustable, it is possible to adjust the gate terminal voltage
of the transistor 633b1, transistor 633b2, and transistor 633b3.
It is possible to adjust the voltage at point a, voltage at
point b, and voltage at point c on a common terminal 1253.
Thus, it is possible to correct (variations in) output current
(programming current) by varying the Vt of the unit transistors
634 in the transistor group 681c1, the Vt of the unit transistors
634 in the transistor group 681c2, and the Vt of the unit
transistors 634 in the transistor group 681cn.

Although three reference current generator circuits are
formed separately in Figure 131, this is not restrictive and
four or more reference current generator circuits may be formed.
They may be constructed of the transistors 633a in the
transistor group 681b shown in Figure 128. By using the
configuration in Figure 128 and controlling (adjusting) the
current passed through the transistors 632a composing current
mirrors, it is possible to simultaneously control (adjust)
the reference currents Ib1, Ib2, and Ib3 shown in Figure 130.
That is, the transistors 633b1, 633b2, and 633b3 are controlled
as a transistor group (see Figure 131(b)).

Figure 130 shows a configuration in which a reference
current regulating means 651a is formed or placed for the
transistor 633b1 and a reference current regulating means 651b
is formed or placed for the transistor 633b2. Figure 132 shows

a configuration in which a source terminal is shared by the
transistors 633b1 and 633b2 and a reference current regulating
means 651 is formed or placed. The reference currents Ib1
and Ib2 are controlled (adjusted) to vary by the current
regulating means 651. The programming current outputted from
the unit transistors 634 varies in proportion to changes in
the reference currents Ib1 and Ib2. The transistor 633b1 and
transistor 633b2 are connected in the same manner as the
transistors 633b in the transistor groups 681c shown in Figure
123.

The reference currents Ib1 and Ib2 are controlled or
adjusted by a reference current regulating means 651 (which,
needless to say, is not limited to a variable regulator, and
may be an electronic regulator). The unit transistors 634
in each transistor group 681c form current mirror circuits
in conjunction with the transistors 633b (633b1 and 633b2).
The reference currents Ib1 and Ib2 define the magnitude of
output current from the unit transistors 634.

With the configuration shown in Figure 129, the reference
current Ib1 is used to adjust mainly the gate terminal voltage
at point a to a predetermined value and reference current Ib2
is used to adjust mainly the gate terminal voltage at point
b to a predetermined value. The reference currents Ib1 and
Ib2 are basically the same current. The transistors 633b1
and 633b2, which are formed close to each other, have an equal

transistor Vt.

Thus, the transistor 633b1 and transistor 633b2 share a gate terminal and the voltages at point a and point b are equal. Consequently, voltage is supplied from both sides of the common terminal 1253, making the voltage at the common terminal 1253 uniform on left and right sides of the IC chip. Once the voltage at the common terminal 1253 is uniform, voltages at the gate terminals of all the unit transistors 634 in the transistor groups 681c become equal. This eliminates variations in the programming current outputted from the unit transistors 634 to the source signal lines 18.

In this way, the configuration in Figure 132 contains two transistors 633b which generate reference current sources. Figure 133 shows a configuration in which gate voltage of a transistor 633b2 constituting a reference current source is applied to the center of the common terminal 1253 as well.

The reference current generator circuit 1 delivers the reference current Ib1 and the reference current generator circuit 2 delivers the reference current Ib2. A reference current generator circuit 3 delivers reference current Ib3. The reference current Ib1, reference current Ib2, and reference current Ib3 have the same current value. The reference currents are controlled or adjusted by a reference current regulating means 651 (which, needless to say, is not limited to a variable regulator, and may be an electronic regulator).

Although three reference current generator circuits are formed separately in Figure 133, this is not restrictive and four or more reference current generator circuits may be formed.

Incidentally, in the configurations in Figures 126, 127, 128, etc., transistors which pass reference currents are placed or formed on both sides of the gate wiring 1261. However, the present invention is not limited to this. Needless to say, a constant voltage may be applied directly to the gate wiring 1261 instead of placing transistors. The above items also apply to other examples of the present invention.

In the above examples, current-based or voltage-based delivery is carried out mainly in a single-stage configuration. However, the present invention is not limited to this. Needless to say, as shown in Figure 146, for example, the present invention is also applicable to a multi-stage configuration shown in Figure 68.

In Figure 147, transistors 631a and 631b are formed or placed on both ends (on or around the left and right ends of an IC chip) of the transistor group 681a. Also, variable resistors 651 are formed or placed as adjusting means of reference currents. Incidentally, the reference currents Ia1 and Ia2 may be fixed. Needless to say, the reference currents Ia1 and Ia2 may be equal.

By adjusting the reference currents Ia1 and Ia2 by the

reference current regulating means 651, it is possible to adjust output current Ib of the transistors 632 in the transistor group 681a. The current Ib is delivered to a transistor 632b, causing a current to flow through the transistors 633a in the transistor groups 681b which form current mirror circuits and thereby determining the output current of the unit transistors 634. Other items are the same as in Figure 68 and the like, and thus description thereof will be omitted.

Although it has been stated that the magnitudes of the reference currents which flow through the transistors placed on both sides of the chip are adjusted by electronic regulators or the like, the present invention is not limited to this. For example, this can be accomplished by trimming reference current adjustment resistors Rm as illustrated in Figure 165. That is, resistance values are increased by trimming the resistors Rm by the laser light 1502 emitted from the laser device 1501. Increasing the resistance values of the resistors Rm changes the reference currents Ia. By trimming resistors Rm1 or Rm2, it is possible to adjust the reference currents Ia1 and Ia2, respectively.

Preferably, the currents generated by the transistors composing current mirror circuits are delivered by a plurality of transistors. Transistors formed in an IC chip 14 have variations in characteristics. To suppress variations in

transistor characteristics, the size of the transistors can be increased. However, if transistor size is increased, the current mirror ratios of the current mirror circuits may deviate. To solve this problem, it is advisable to make current- or voltage-based delivery using a plurality of transistors. The use of multiple transistors decreases overall variations even if there are variations in the characteristics of individual transistors. This also improves the accuracy of current mirror ratios. All in all, the area of the IC chip is reduced as well. Figure 156 shows an example. Incidentally, the above items apply to both current-based or voltage-based multi-stage delivery and current-based or voltage-based single-stage delivery.

In Figure 156, the transistor group 681a and transistor groups 681b compose current mirror circuits. The transistor group 681a consists of a plurality of transistors 632b. On the other hand, each of the transistor groups 681b consists of a plurality of transistors 633a. Similarly, each of the transistor groups 631c consists of a plurality of transistors 633c.

The transistor group 681b1, transistor group 681b2, transistor group 681b3, transistor group 681b4, and so on are composed of the same number of transistors 633a. Also, the total area of the transistors 633a is (approximately) equal

among the transistor groups 681b (where the total area is the W and L sizes of the transistors 633a in each transistor group 681b multiplied by the number of the transistors 633a). The same applies to the transistor groups 681c.

Let Sc denote the total area of the transistors 633b in each transistor group 681c (where the total area is the W and L sizes of the transistors 633b in each transistor group 681c multiplied by the number of the transistors 633b). Also, let Sb dente the total area of the transistors 633a in each transistor group 681b (where the total area is the W and L sizes of the transistors 633a in each transistor group 681b multiplied by the number of the transistors 633a). Also, let Sa dente the total area of the transistors 632b in each transistor group 681a (where the total area is the W and L sizes of the transistors 632b in the transistor group 681a multiplied by the number of the transistors 632b). Also, let Sd dente the total area of the unit transistors 634 per output.

Preferably, the total area Sc and the total area Sb are approximately equal. Also, it is preferably that the transistors 633a composing each transistor group 681b and the transistors 633b composing each transistor group 681c are equal in number. However, considering layout constraints on the IC chip 14, the transistors 633a composing each transistor group 681b may be made smaller in number and larger in size than the transistors 433b composing each transistor group 681c.

An example of the above configuration is shown in Figure 157. The transistor group 681a consists of a plurality of transistors 632b. The transistor group 681a and transistors 633a compose a current mirror circuit. The transistors 633a generates current Ic. One transistor 633a drives a plurality of transistors 633b in a transistor group 681c (the current Ic from the single transistor 633a is shunted to the plurality of transistors 633b . Generally, the number of transistors 633a corresponds to the number of output circuits. For example, in a QCIF+ panel, there are 176 transistors 633a in each of R, G, and B circuits.

The relationship between the total area Sd and total area Sc is correlated with output variations. This correlation is shown in Figure 210. For a variation rate and the like, refer to Figure 170. The variation rate when total area Sd : total area Sc = 2 : 1 (Sc/Sd = 1/2) is taken as 1. As can bee seen from Figure 210, a small Sc/Sd ratio results in a sharp deterioration in the variation rate. A poor variation rate results especially when Sc/Sd is 1/2 or less. Output variations decrease when Sc/Sd is 1/2 or above. The decrease is gradual. Output variations fall within an allowable range when Sc/Sd is around 1/2 or larger. In view of the above circumstances, it is preferable that $1/2 \leq$ Sc/Sd is satisfied. However, a larger Sc means a larger IC chip. Thus, an upper

limit of Sc/Sd = 4 should be provided.   That is, a relationship
$1/2 \leq$ Sc/Sd ≤ 4 should be satisfied.

Incidentally, $A \geq B$ means that A is equal to or larger
than B. $A > B$ means that A is larger than B. $A \leq B$ means
that A is equal to or smaller than B. $A < B$ means that A is
smaller than B.

Besides, preferably the total area Sd and total area Sc
are approximately equal.   Furthermore, preferably the number
of the unit transistors 634 per output and the number of the
transistors 633b in each transistor group 681c are equal.   That
is, in the case of 64 gradations, there are 63 unit transistors
634 per output.   Thus, there are 63 transistors 633b in the
transistor group 681c.

Also, preferably the transistor group 681a, transistor
groups 681b, and the transistor groups 681c are composed of
unit transistors 634 whose WL area is within a factor of four.
More preferably, they are composed of unit transistors 484
whose WL area is within a factor of two.   Even more preferably,
they are composed of unit transistors 484 of the same size.
That is, current mirror circuits and the output current circuit
704 are composed of transistors of approximately the same size.

The total area Sa should be larger than the total area
Sb.   Preferably, a relationship 200 Sb $\geq$ Sa ≥ 4 Sb is satisfied.
Also, the total area Sa of the transistors 663a composing all

the transistor groups 681b should be approximately equal to Sa.

Incidentally, as illustrated in Figure 164, the transistor 632a which forms current mirror circuits in conjunction with the transistor groups 681b does not need to be included in the transistor group 681a (see Figure 156).

In the configuration in Figures 126, 127, 128, 147, or the like, transistors which pass reference currents are placed or formed on both sides of the gate wiring 1261. Figure 158 shows an example in which this configuration (scheme) is applied to the configuration in Figure 157. In Figure 158, transistor groups 681a1 and 681a2 are placed or formed on both sides of the gate wiring 1261. Other items are the same as in Figure 126, 127, 128, 147, etc. and thus description thereof will be omitted.

In the configuration shown in Figures 126, 127, 128, 147, 158, etc., a transistor or transistor group is placed at each end of the gate wiring 1261. Thus, a total of two transistors or two transistor groups are placed at both ends of the gate wiring 1261. However, the present invention is not limited to this. As illustrated in Figure 159, a transistor or transistor group may be placed at the center or other location of the gate wiring 1261. Three transistor groups 681a are formed in Figure 159. The present invention is characterized in that a plurality of transistors or transistor groups 681

are formed on the gate wiring 1261. The use of multiple transistors or transistor groups makes it possible to reduce the impedance of the gate wiring 1261, resulting in improved stability.

To further improve the stability, it is preferable to form or place a capacitor 1601 on the gate wiring 1261 as illustrated in Figure 160. Alternatively, the capacitor 1601 may be formed in the IC chip 14 or source driver circuit 14 or placed or mounted outside the chip as an external capacitor of the IC 14. When mounting the capacitor 1601 externally, a capacitor connection terminal is placed on an IC chip terminal.

The above example is configured to pass a reference current, copy the reference current using a current mirror circuit, and transmit the reference current to the unit transistor 634 in the final stage. When the image display is black display (complete black raster), current does not flow through any unit transistor 634 because every switch 641 is open. Thus, 0 (A) current flows through the source signal line 18, consuming no power.

However, even during black raster display, reference currents flow. Examples include the current Ib and Ic in Figure 161. They become reactive currents. Reference currents flow efficiently if configured to flow during current programming. Thus, the flow of reference current is limited during vertical

and horizontal blanking periods of images. Also, the flow of reference current is limited during wait periods.

To prevent reference current from flowing, a sleep switch 1611 can be opened as shown in Figure 161. The sleep switch 1611 is an analog switch. The analog switch is formed in the source driver circuit or source driver IC 14. Of course, the sleep switch 1611 may be placed outside the IC 14 and controlled.

When the sleep switch 1611 is turned off, the reference current Ib stops flowing. Consequently, current does not flow through the transistors 633a in a transistor group 681a1, and the reference current Ic is also reduced to 0 A. Thus, current does not flow through the transistors 633b in a transistor group 681c either. This improves power efficiency.

Figure 162 is a timing chart. A blanking signal is generated in sync with a horizontal synchronization signal HD. The period when the blanking signal is high corresponds to a blanking period. When the blanking signal is low, a video signal is being applied. The sleep switch 1611 is off (open) when the blanking signal is low, and on when the signal is high.

During a blanking period A when the sleep switch 1611 is off, reference current does not flow. During a period D when the sleep switch 1611 is on, the reference current flows.

Incidentally, on/off control of the sleep switch 1611 may be performed according to image data. For example, when

all image data in a pixel row is black image data (for a period
of 1 H, the programming currents outputted to all source signal
lines 18 are 0), the sleep switch 1611 is turned off to stop
reference currents (Ic, Ib, etc.) from flowing. Also, a sleep
switch may be formed or placed for each source signal line
and be subjected to on/off control. For example, when an
odd-numbered source signal line 18 is in black display mode
(vertical black stripe display), the corresponding sleep
switch is turned off.

With the configuration shown in Figure 124, the reference
current Ib flows through the transistor 633 during a video
period. The switches 641 are turned on and off according to
image data and current flows through the appropriate unit
transistors 634. All the switches 641 are open during black
raster display. Even if the switches 641 are open, since the
reference current Ib flows through the transistor 633, the
unit transistors 634 try to pass current. This lowers
inter-channel voltage (Vsd) of the unit transistors 634
(eliminates potential difference between source potential and
drain potential). The potential of the gate wiring 1261 of
the unit transistors 634 also drops at the same time.
When an image changes from black raster to white raster, the
switches 641 are turned on, developing the voltage Vsd in the
unit transistors 634. There is a parasitic capacitance
between the gate wiring 1261 and internal wiring 643 (the source

signal line 18).

The parasitic capacitance between the gate wiring 1261 and internal wiring 643 (the source signal line 18) in conjunction with the Vsd in the unit transistors 634 causes potential fluctuations in the gate wiring 1261.
The potential fluctuations cause changes to the output current of the unit transistors 634. The changes in the output current produce horizontal streaks and the like in images. The horizontal streaks appear where the images change from white display to black display or from black display to white display.

Figure 151 illustrates potential fluctuations in the gate wiring 1261. Linking occurs at image change points (where the images change from white display to black display, from black display to white display, etc.).

Figure 152 shows a method of solving this problem. Resistors R are formed or placed in the selector switches 641. Specifically, sizes of the analog switches 641 are changed instead of forming the resistors R. Thus, Figure 152 is an equivalent circuit diagram of the switches 641.

The resistors in the switches 641 are designed to satisfy the following relations.

R1 < R2 < R3 < R4 < R5 < R6

D0 is provided by 1 unit transistor 634. D1 is provided by 2 unit transistors 634. D2 is provided by 4 unit transistors 634. D3 is provided by 8 unit transistors 634. D4 is provided

by 16 unit transistors 634. D5 is provided by 32 unit
transistors 634. Thus, the current flowing through the
switches 641 increases with changes from D0 to D5. It is also
necessary to lower the on-resistance of the switches
accordingly. On the other hand, it is also necessary to reduce
linking as illustrated in Figure 151. The configuration shown
in Figure 152 makes it possible to reduce linking and adjust
the on-resistance of the switches.

The linking of the gate wiring 1261 in Figure 151 is caused
by existence of an image which turns off all the unit transistors
634 and flow of the reference current Ib while all the unit
transistors 634 are off (see Figure 153 and the like).
For the above reasons, the gate wiring of the unit transistors
634 is prone to potential fluctuations.

Figure 127 and the like show configuration which contain
multi-stage current mirror connections. Figures 129 to 133
show single-stage configurations. The problem of swinging
gate wiring 1261 has been described with reference to Figure
151. The swing is influenced by the power supply voltage
of the source driver IC 14 because the power supply voltage
swings to a maximum voltage. Figure 211 shows a ratio of
potential fluctuations of the gate wiring based on the value
obtained when the power supply voltage of the source driver
IC 14 is 1.8 V. The fluctuation ratio increases with increases
in the power supply voltage of the source driver IC 14. An

allowable range of fluctuation ratio is approximately 3. A
higher fluctuation ratio will cause horizontal cross-talk.
The fluctuation ratio with respect to the power supply voltage
tends to increase when the power supply voltage of the IC is
10 to 12 V or higher. Thus, the power supply voltage of the
source driver IC 14 should be 12 V or less.

On the other hand, in order for a driver transistor 11a
switch from white-display current to black-display current,
it is necessary to make a certain amplitude change to the
potential of the source signal line 18. The required range
of amplitude change is 2.5 V or more. It is lower than the
power supply voltage because the output voltage of the source
signal line 18 cannot exceed the power supply voltage.

Thus, the power supply voltage of the source driver IC
14 should be from 2.5 V to 12 V (both inclusive). The use
of this range makes it possible to keep fluctuations in the
gate wiring 1261 within a stipulated range, eliminate
horizontal cross-talk, and thus achieve proper image display.

Wiring resistance of the gate wiring 1261 also presents
a problem. In Figure 215, the wiring resistance (Ω) of the
gate wiring 1261 is the resistance of the wiring throughout
its length from transistor 633b1 to transistor 633b2 or the
resistance of the gate wiring throughout its length. The
magnitude of a transient phenomenon as shown in Figure 151
depends on one horizontal scanning period (1 H) as well because

the shorter the period of 1 H, the larger the impact of the transient phenomenon. A larger wiring resistance (Ω) makes a transient phenomenon as shown in Figure 151 easier to occur. This phenomenon poses a problem especially for the configurations of single-stage current-mirror connections shown in Figures 129 to 133, and 215 to 220 in which the gate wiring 1261 is long and connected with a large number of unit transistors 634.

Figure 212 is a graph in which the horizontal axis represents the product (R·T) of wiring resistance (Ω) of the gate wiring 1261 and 1-H period T (sec) while the vertical axis represents a fluctuation ratio. The fluctuation ratio is taken as 1 when R·T = 100. As can be seen from Figure 212, fluctuation ratio tends to grow larger when R·T is 5 or less. Fluctuation ratio also tends to grow larger when R·T is 1000 or more. Thus, it is preferable that R·T is from 5 to 100 (both inclusive).

Another method of solving this problem is shown in Figure 153. In Figure 153, the unit transistors 1531 which pass current steadily are formed or placed. These transistors 1531 are referred to as steady-state transistors 1531.

The steady-state transistors 1531 pass current Is constantly while the reference current Ib is flowing. Thus, they do not depend on the magnitudes of the programming current Iw. The flow of the current Is reduces potential

fluctuations of the gate wiring 1261. Preferably, the current Is is from 2 to 8 times (both inclusive) as large as the current flowing through the unit transistors 634. The steady-state transistors 1531 are constructed of multiple transistors with the same WL as the unit transistors 634. Also, preferably the steady-state transistors 1531 are formed at a location farthest from the transistor 633 which passes the reference current Ib.

Although it has been stated with reference to Figure 153 that multiple steady-state transistors 1531 are formed, the present invention is not limited to this. A single steady-state transistor 1531 may be formed as shown in Figure 155. Also, steady-state transistors 1531 may be formed at multiple locations as shown in Figure 154. In Figure 154, one steady-state transistor 1531a is formed near the transistor 633 and four steady-state transistors 1531b are formed at a location farthest from the transistor 633.

In Figure 154, a switch S1 is formed for the steady-state transistors 1531b. The switch S1 is turned on and off according to image data (D0 to D5). In the case of black raster image data (including image data close to black raster (higher-order bits of D are 0)), output of a NOR circuit 1541 goes high, the switch S1 turns on, and a current Is2 flows through the steady-state transistors 1531. Otherwise, the switch S1 remains off and current does not flow through the steady-state

transistors 1531. This configuration can reduce power consumption.

Figure 163 shows a configuration which includes both the steady-state transistors 1531 and sleep switch 1611. Thus, needless to say, what has been described herein can be used in combination.

Dummy transistor groups 681c are formed or placed on outer sides of the transistor groups 681c1 and 681cn located on both ends of the chip IC. Preferably, at least two dummy transistor groups 681c are formed on the left and right (outermost sides) of the chip IC. More preferably, three to six circuits (both inclusive) are formed. Without dummy transistor groups 681c, a diffusion process or etching process during production of the IC will cause the unit transistors 634 in outer transistor groups 681c to differ in Vt from those in the center of the IC chip 14. Difference in the Vt will cause variations in the output current (programming current) of the unit transistors 634.

Figures 129 to 133 are block diagrams of a driver IC with a single-stage current mirror configuration. The single-stage configuration will be described further. Figure 215 shows a single-stage driver circuit configuration. The transistor groups 681c in Figure 215 correspond to an output stage configuration consisting of the unit transistors 634 shown in Figure 214 (see also Figures 129 to 133).

The transistor 632b and two transistors 633a compose a current mirror circuit. The transistor 633a1 and transistor 633a2 are of the same size. Thus, current Ic passed by the transistor 633a1 and current Ic passed by the transistor 633a2 are identical.

In Figure 214, the transistor groups 681c consisting of unit transistors 634 compose current mirror circuits together with the transistor 633b1 and transistor 633b2. There are variations in the output current of the transistor groups 681c. However, transistor groups 681 which compose a current mirror circuit in close vicinity to each other have their output current controlled accurately. The transistor 633b1 and transistor group 681c1 compose a current mirror circuit in close vicinity to each. Also, The transistor 633b2 and transistor group 681cn compose a current mirror circuit in close vicinity to each. If the current flowing through the transistor 633b1 and the current flowing through the transistor 633b2 are equal, the output current of the transistor group 681c1 and the output current of the transistor group 681cn are equal. If the current is generated in each IC chip accurately, the output currents of the transistor groups 681c at both ends of the output stage are equal in any IC chip. Thus, even if IC chips are cascaded, seams between ICs can be made inconspicuous.

As is the case with Figure 123, a plurality of transistors 633b may be provided to form a transistor group 681b1 and transistor 681b2. Also, a plurality of transistors 633a may be provided to form a transistor group 681a as in Figure 123.

Although it has been stated that the transistor 632b current is specified by the resistance R1, this is not restrictive. Electronic regulators 1503a and 1503b may be used as shown in Figure 218. In the configuration shown in Figure 218, the electronic regulators 1503a and 1503b can be operated independently. Thus, the values of the currents flowing through the transistors 632a1 and 632a2 can be changed. This makes it possible to adjust the slopes of the output currents in output stages 681c on the left and right sides of the chip. Incidentally, it is also possible to provide only one electronic regulator 1503 as shown in Figure 219 and use it to control two operational amplifiers 722.

The sleep switch 1611 has been described with reference to Figure 161. Needless to say, a sleep switch may be placed or formed similarly as shown in Figure 220. In Figures 153, 154, 155, and 163, it has been stated that the steady-state transistors 1531 are formed or placed, and the steady-state transistors 1531 in Figure 226(b) may be formed or placed in block A as illustrated in Figure 225.

Also, it has been stated with reference to Figure 160 that the capacitor 1601 is connected to the gate wiring 1261

for stability, and it goes without saying that the stabilizing capacitor 1601 in Figure 226(a) may be placed in the block A in the Figure 225 as well.

Also, it has been stated with reference to Figure 165 and the like that resistors and the like are trimmed for adjustment of current. Similarly, needless to say, the resistor R1 or R2 may be trimmed as illustrated in Figure 225.

It has been stated with reference to Figure 210 that there are conditions for the area in which the transistor groups 681 are constructed. However, the conditions in Figure 210 do not apply to the single-stage current mirror configurations in Figures 129 to 133 and Figures 215 to 220, in which there are a very large number of unit transistors 634. An output stage of a single-stage driver circuit will be described additionally below. Incidentally, for ease of explanation, Figures 216 and 217 will be taken as an example. However, since the description concerns the number and total area of transistors 633b as well as the number and total area of unit transistors 634, it goes without saying that the description applies to other examples as well.

Figures 216 and 217, let Sb denote the total area of the transistors 633b in each transistor group 681b (where the total area is the W and L sizes of the transistors 633b in each transistor group 681b multiplied by the number of the transistors 633b). Incidentally, if transistor groups 681b

are installed on the left and right of the gate wiring 1261 as in Figures 216 and 217, the area is doubled. If there is one transistor as shown in Figure 129, Sb equals the area of the transistor 633b. If the transistor group 681b consists of a single transistor 633b, needless to say, Sb equals the size of the one transistor 633b.

Also, let Sc denote the total area of the unit transistors 634 in each transistor group 681c (where the total area is the W and L sizes of the transistors 634 in each transistor group 681c multiplied by the number of the transistors 634). It is assumed that the number of the transistor groups 681c is n. In the case of a QCIF+ panel, n is 176 (a reference current circuit is formed for each of R, G, and B).

In Figure 213, the horizontal axis represents Sc × n/Sb and the vertical axis represents a fluctuation ratio. The fluctuation ratio in the worst case is taken as 1. As illustrated in Figure 213, the fluctuation ratio deteriorates with increases in Sc × n/Sb. A large value of Sc × n/Sb means that the total area of the unit transistors 634 in the transistor groups 681c is larger than the total area of the transistors 633b in the transistor groups 681b when the number n of output terminals is constant. In that case, the fluctuation ratio is unfavorable.

A small value of Sc × n/Sb means that the total area of the unit transistors 634 in the transistor groups 681c is

smaller than the total area of the transistors 633b in the transistor groups 681b when the number n of output terminals is constant. In that case, the fluctuation ratio is small.

An allowable range of fluctuations corresponds to a value of Sc × n/Sb of 50 or less. When Sc × n/Sb is 50 or less, the fluctuation ratio falls within the allowable range and potential fluctuations of the gate wiring 1261 is extremely small. This makes it possible to eliminate horizontal cross-talk, keep output variations within an allowable range, and thus achieve proper image display. It is true that the fluctuation ratio falls within the allowable range when Sc × n/Sb is 50 or less. However, decreasing Sc × n/Sb to 5 or less has almost no effect. On the contrary, Sb becomes large, increasing the chip area of the IC 14. Thus, preferably Sc × n/Sb to 5 should be from 5 to 50 (both inclusive).

Also, placement of unit transistors 634 in the transistor groups 681c has consideration.
The transistor groups 681c should be placed orderly.
Any dropout of a unit transistor 634 will make the characteristics of the unit transistors 634 around it different from the characteristics of the other unit transistors 634.

Figure 134 schematically illustrates an arrangement of the unit transistors 634 in the transistor groups 681c in the output stage. Sixty-three (63) unit transistors 634 which represent 64 gradations are arranged orderly in a matrix.

However, although 64 unit transistors 634 could be arranged in 4 rows × 16 columns, arrangement of 63 unit transistors 634 produces a vacancy (shaded area). This makes the characteristics of the unit transistors 634a, 634b, and 634c around the shaded area different from the characteristics of the other unit transistors 634.

To solve this problem, the present invention forms or places a dummy transistor 1341 in the shaded area. This makes the characteristics of the unit transistors 634a, 634b, and 634c coincide with the characteristics of the other unit transistors 634. That is, by forming the dummy transistors 1341, the present invention arranges the unit transistors 634 in a matrix. Also, the unit transistors 634 are arranged in a matrix without any omission. Also, the unit transistors 634 are arranged axisymmetrically.

Although it has been stated that 63 unit transistors 634 are arranged in each transistor group 681c to represent 64 gradations, the present invention is not limited to this. The unit transistor 634 may be further composed of a plurality of sub-transistors.

Figure 135(a) shows the unit transistor 634. Figure 135(b) shows a unit transistor (single unit) 1351 composed of four sub-transistors 1352. The unit transistor (single unit) 1351 is designed to be equal in output current to the unit transistor 634. That is, the unit transistor 634 is

composed of four sub-transistors 1352. Incidentally, the
present invention is not limited to a configuration in which
the unit transistor 634 is composed of four sub-transistors
1325, and is applicable to any configuration in which the unit
transistor 634 is composed of multiple sub-transistors 1352.
However, the sub-transistors 1352 are designed to be of the
same size or to produce the same output current.

In Figure 135, reference character S denotes the source
terminal of a transistor, G denotes the gate terminal of the
transistor, and D denotes the drain terminal of the transistor.
In Figure 135(b), the sub-transistors 1352 are oriented in
the same direction. In Figure 135(c), the sub-transistors
1352 are oriented differently between different rows.
In Figure 135(d), the sub-transistors 1352 are oriented
differently between different columns and arranged
symmetrically about a point. All the arrangements in Figures
135(b), 135(c), and 135(d) have regularities.

Changes in the formation direction of the unit transistors
634 or sub-transistors 1352 often change their characteristics.
For example, in Figure 135(c), the unit transistor 634a and
sub-transistor 1352b produce different output currents even
if an equal voltage is applied to their gate terminals.
However, in Figure 135(c), sub-transistors 1352 with different
characteristics are formed in equal numbers. This reduces
variations in the transistor (unit) as a whole. If the

orientations of unit transistors 634 or sub-transistors 1352 with different formation directions are changed, differences in characteristics will complement each other, resulting in reduced variations in the transistor (single unit). Needless to say, the above items also apply to the arrangement in Figure 135(d).

Thus, as illustrated in Figure 136 and the like, by changing the orientations of unit transistors 634, it is possible to cause the characteristics of the unit transistors 634 formed in the vertical direction and the characteristics of the unit transistors 634 formed in the horizontal direction to complement each other in the transistor groups 681c as a whole, resulting in reduced variations in the transistor groups 681c as a whole.

Figure 136 shows an example in which the unit transistors 634 are oriented differently between different columns within each transistor groups 681c. Figure 137 shows an example in which the unit transistors 634 are oriented differently between different rows within each transistor groups 681c. Figure 138 shows an example in which the unit transistors 634 are oriented differently between different rows as well as between different columns within each transistor group 681c. Incidentally, these requirements are also observed when forming or placing a dummy transistor 1341.

The above examples involve constructing or forming unit

transistors of the same size or same current output in the transistor groups 681c (see Figure 139(b)). However, the present invention is not limited to this. A configuration illustrated in Figure 139(a) may also be used as follows. A single-unit unit transistor 634a is connected (formed) for the 0th bit (switch 641a). A 2-unit unit transistor 634b is connected (formed) for the 1st bit (switch 641b). A 4-unit unit transistor 634c is connected (formed) for the 2nd bit (switch 641c). An 8-unit unit transistor 634d is connected (formed) for the 3rd bit (switch 641d). A 16-unit unit transistor 634a is connected (formed) for the 4th bit (not shown). A 32-unit unit transistor 634a is connected (formed) for the 5th bit (not shown). Incidentally, a 16-unit unit transistor, for example, is a transistor which outputs current equivalent to the current outputted by 16 unit transistors 634.

An n-unit (n is an integer) unit transistor can be formed easily by changing the channel width W proportionally (while keeping the channel length L constant). Actually, however, doubling the channel width W often does not double the output current. Thus, the channel width W is determined experimentally by actually building transistors. According to the present invention, however, even if the channel width W deviates more or less from proportionality, it is assumed that the channel width W is proportional.

Reference current circuits will be described below. Output current circuits 704 are formed (placed) individually for R, G, and B. The RGB output current circuits 704R, 704G, and 704B are placed in close vicinity. Also, a reference current INL in a low-current region in Figure 73 and reference current INH in a low-current region in Figure 74 are adjusted to each color (R, G, and B) (see also Figure 79).

Thus, an output current circuit 704R for R is equipped with a regulator (or an electronic regulator for voltage output or current output) 651RL to adjust the reference current INL in the low-current region and a regulator (or an electronic regulator for voltage output or current output) 651RH to adjust the reference current INH in the high-current region. Similarly, an output current circuit 704G for G is equipped with a regulator (or an electronic regulator for voltage output or current output) 651GL to adjust the reference current INL in the low-current region and a regulator (or an electronic regulator for voltage output or current output) 651GH to adjust the reference current INH in the high-current region. Also, an output current circuit 704B for B is equipped with a regulator (or an electronic regulator for voltage output or current output) 651BL to adjust the reference current INL in the low-current region and a regulator (or an electronic regulator for voltage output or current output) 651BH to adjust the reference current INH in the high-current region.

Preferably, the regulators 651 and the like should be capable of accommodating temperature changes to compensate for temperature characteristics of the EL element 15. Needless to say, if there are two or more breakpoints in gamma characteristics shown in Figure 79, three or more electronic regulators or resistors may be provided to adjust the reference currents for the different colors.

Output pads 761 are formed or placed on the output terminals of the IC chip. They are connected with the source signal lines 18 of the display panel. A bump is formed on the output pads 761 by a plating technique or ball bonding technique. The bump should be 10 to 40 μm high (both inclusive).

The bumps and the source signal lines 18 are connected electrically via a conductive bonding layer (not shown). The conductive bonding layer is made of an epoxy or phenolic base resin mixed with flakes of silver (Ag), gold (Au), nickel (Ni), carbon (C), tin oxide (SnO2), and the like, or made of an ultraviolet curing resin. The conductive bonding layer is formed on the bump by a transfer or other technique. Also, the bumps and the source signal lines 18 are bonded by thermocompression using an ACF resin. Incidentally, the techniques for connecting the bumps or output pads 761 with the source signal lines 18 are not limited to those described above. Besides, a film carrier technique may be used instead

of mounting the IC 14 on the array board. Also, polyimide films and the like may be used for connection with the source signal lines 18 and the like.

Referring to Figure 69, inputted 4-bit current control data (DI) is decoded by a 4-bit decoder circuit 692 (needless to say, a 6-bit decoder circuit is used if there are 64 divisions. For ease of explanation, it is assumed here that 4-bit data is used). Decoder output is boosted from logic level voltage value to analog level voltage value by a level shifter circuit 693 and is entered into the analog switch 641.

Main components of an electronic regulator circuit are a fixed resistor R0 (691a) and 16 unit registers r (691b). Output from the decoder circuit 692 is connected to one of 16 analog switches 641 and designed to determine the resistance value of the electronic regulator by the output from the decoder circuit 692. For example, if an output of the decoder circuit 692 is 4, the resistance value of the electronic regulator is R0 + 5r. The resistance value of the electronic regulator acts as a load on the first-stage current source 631 and is pulled up to an analog power supply AVdd. Thus, changes in the resistance value of the electronic regulator cause changes to the current value of the first-stage current source 631. This in turn causes changes to the current value of the second-stage current source 632, consequently causing changes to the current value of the third-stage current source 633.

The output current of the driver IC is controlled in this way.

Incidentally, although it has been assumed for the sake of illustration that 4-bit data is used for current value control, this is not restrictive. Needless to say, the larger the bit count, the larger the number of steps of current. Also, although it has been stated that the multi-stage current mirrors have a three-stage configuration, needless to say, this is not restrictive and any number of stages may be used.

Besides, to deal with the problem of changes in emission brightness of the EL element caused by temperature changes, preferably the electronic regulator circuit is equipped with an external resistor 691a whose resistance changes with temperature. Figures 33 and 35 and the like xternal resistors whose resistance changes with temperature include, for example, thermistors, posistors, etc. Generally, light-emitting elements whose brightness varies with the current flowing through themselves have temperature dependence and their emission brightness varies with temperature even if a current of the same value is passed through them. By attaching an external resistor 691a whose resistance changes with temperature to an electronic regulator, it is possible to vary the current value of constant-current output with temperature and keep the emission brightness constant even if the temperature changes.

Preferably, the multi-stage current mirror circuits are

divided into three systems for red (R), green (G), and blue (B). Generally, organic EL or other current-driven light-emitting elements have different emission characteristics among R, G, and B. Thus, to obtain the same brightness among R, G, and B, the currents passed through the light-emitting elements should be adjusted separately for R, G, and B. Also, current-driven light-emitting elements such as for organic EL display panel have different temperature characteristics among R, G, and B. Thus, characteristics of auxiliary elements such as thermistors formed or placed to compensate for temperature characteristics should also be adjusted separately for R, G, and B.

Since the multi-stage current mirror circuits are divided into three systems for red (R), green (G), and blue (B), the present invention makes it possible to adjust emission characteristics and temperature characteristics separately for R, G, and B, and thereby obtain an optimum white balance.

As described earlier, in the case of current driving, only a small current is written into pixels during black display. Consequently, if the source signal lines 18 or the like have parasitic capacitance, current cannot be written into the pixels 16 sufficiently during one horizontal scanning period (1 H). Generally, in current-driven light-emitting elements, black-level current is as weak as a few nA, and thus it is difficult to drive parasitic capacitance (load capacitance

of wiring) which is assumed to measure tens of pF using the signal value of the black-level current. To solve this problem, it is useful to equalize the black-level current in the pixel transistors 11a (basically, the transistors 11a are off) with the potential level of the source signal lines 18 by applying a precharge voltage before writing image data into the source signal lines 18. In order to form (create) the precharge voltage, it is useful to output the black level at a constant voltage by decoding higher order bits of image data.

Figure 70 shows an example of a current-output type source driver circuit (IC) 14 equipped with a precharge function according to the present invention. Figure 70 shows a case in which the precharge function is provided in the output stage of a 6-bit constant-current output circuit. In Figure 70, a precharge control signal is constituted so that it decodes the case where the higher order three bits D3, D4, and D5 in image data D0 to D5 are all zero by a NOR circuit 702, takes an AND circuit 703 with an output from a counter circuit 701 of a dot clock CLK with a reset function based on a horizontal synchronization signal HD, and thereby outputs a black level voltage Vp for a fixed period. In other cases, an output current from the current output stage 704 described with reference to Figure 68, etc. is applied to the source signal lines 18 (programming current Iw is drawn from the source signal lines 18). When the image data is composed of the 0th to 7th

gradations close to the black level, by writing a voltage which corresponds to the black level only for a fixed period at the beginning of a horizontal period, the above configuration reduces the burden of current driving and makes up for insufficient writing. Incidentally, it is assumed that the 0th gradation corresponds to a completely black display while the 63rd gradation corresponds to a completely white display (in the case of 64-gradation display).

Preferably, gradations for which precharging is performed should be limited to a black display region. Specifically, precharging is performed by selecting gradations in a black region (low brightness region, in which only a small (weak) write current flows in the case of current driving) from write image data (selective precharging). If precharging is performed over the entire range of gradations, brightness lowers (a target brightness is not reached) in a white display region. Also, vertical streaks may be displayed in some cases.

Preferably, selective precharging is performed for 1/8 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the 0th to 7th gradations). More preferably, selective precharging is performed for 1/16 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for

the 0th to 3rd gradations).

A method which performs precharging by detecting only the 0th gradation is also effective in enhancing contrast, especially in black display. It achieves an extremely good black display. The problem is that the screen appears whitish in hue when the entire screen displays the 1st and second gradations. Thus, selective precharging is performed in a predetermined range: 1/8 of all the gradations beginning with the 0th gradation. The method of performing precharging by extracting only the 0th gradation causes little harm to image display. Thus, it is most preferable to adopt this method as a precharging technique.

Incidentally, it is also useful to vary the precharge voltage and gradation range among R, G, and B because emission start voltage and emission brightness of EL elements 15 vary among R, G, and B. For example, selective precharging is performed for 1/8 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the 01th to 7th gradations) in the case of R. In the case of other colors (G and B), selective precharging is performed for 1/16 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the 0th to 3rd gradations). Regarding the precharge voltage, if 7 V is written into the source signal lines 18 for R, 7.5 V

is written into the source signal lines 18 for the other colors (G and B). Optimum precharge voltage often varies with the production lot of the EL display panel. Thus, preferably precharge voltage is adjustable with an external regulator or the like. Such a regulator circuit can be also implemented easily using an electronic regulator circuit.

Incidentally, it is preferable that the precharge voltage is not higher than the anode voltage Vdd minus 0.5 V and within the anode voltage Vdd minus 2.5 V in Figure 1.

Even with methods which perform precharging only for the 0th gradation, it is useful to perform precharging selecting one or two colors from among R, G, and B. This will cause less harm to image display.

It is preferable to provide several modes which can be switched by command: including a 0th mode in which no precharging is performed, first mode in which precharging is performed only for the 0th gradation, second mode in which precharging is performed in the range of the 0th to 3rd gradations, third mode in which precharging is performed in the range of the 0th to 7th gradations, and fourth mode in which precharging is performed in the entire range of gradations and the like. These modes can be implemented easily by constructing (designing) a logic circuit in the source driver circuit (IC) 14.

Figure 75 is a diagram showing a concrete configuration

of a selective precharging circuit.

Reference character PV denotes an input terminal of precharge voltage. Separate precharge voltages are set for R, G, and B by external inputs or by an electronic regulator circuit. Incidentally, although it has been stated that separate precharge voltages are set for R, G, and B, this is not restrictive. Precharge voltages may be common to R, G, and B because they are correlated with the Vt of the driver transistors 11a of the pixels 16, which do not differ among R, G, and B. If the W/L ratio and the like of the driver transistors 11a of the pixels 16 are varied (designed differently) among R, G, and B, preferably the precharge voltage is adjusted to the different designs. For example, a larger channel length L of the driver transistor 11a lowers diode characteristics of the transistor 11a and increases the source-drain (SD) voltage. Thus, the precharge voltage should be set lower than the source potential (Vdd).

The precharge voltage PV is fed to an analog switch 731. To reduce on-resistance, the W (channel width) of the analog switch 731 should be 10 μm or above. However, it is set to 100 μm or below because too large W will increase parasitic capacitance as well. More preferably, the channel width W should be between 15 μm and 60 μm (both inclusive). The above items also apply to the analog switch 731 in the switch 641b in Figure 75 and to the analog switch 731 in Figure

73.

The switch 641a is controlled by a precharge enable (PEN)
signal, selective precharging (PSL) signal, and the higher
order three bits (H5, H4, and H3) of the logic signal in Figure
74. The higher order three bits (H5, H4, and H3) of the logic
signal are cited because selective precharging is performed
when they are "0." That is, precharging is performed
selectively when the lower order three bits are "1" (from the
0th to the 7th gradation).

Incidentally, although selective precharging may be
performed for fixed gradations such as only the 0th gradation
or a range of the 0th to 7th gradations, it may be performed
automatically in any low gradation region specified (gradation
0 to gradation R1 or gradation "R1 - 1" in Figure 79).
Specifically, if a low gradation region ranging from gradation
0 to gradation R1 is specified, selective precharging will
be performed automatically in this range, and if a low gradation
region ranging from gradation 0 to gradation R2 is specified,
selective precharging will be performed automatically in this
range. This control system requires a smaller hardware scale
than other systems.

The switch 641a is turned on or off depending on which
of the above signals is applied. When the switch 641a is on,
the precharge voltage PV is applied to the source signal line
18. Incidentally, the time during which the precharge voltage

PV is applied is set by a counter (not shown) formed separately. The counter is configured to be set by command. Preferably, the application duration of the precharge voltage is from 1/100 to 1/5 of one horizontal scanning period (1 H) both inclusive. For example, if 1 H is 100 μsec, the application duration should be from 1 μsec to 20 μsec (from 1/100 to 1/5 of 1 H) both inclusive. More preferably, it should be from 2 μsec to 10 μsec (from 2/100 to 1/10 of 1 H) both inclusive.

Figure 173 shows a variation of Figure 70 or 75. It shows a precharge circuit which determines whether to perform precharging according to input image data and controls precharging. For example, the precharge circuit can make a setting so as to perform precharging when image data contains only the 0th gradation, perform precharging when image data contains only the 0th and 1st gradations, or always perform precharging when the 0th gradation occurs and perform precharging when the 1st gradation occurs consecutively for or beyond a predetermined number of times.

Figure 173 shows an example of a current-output type source driver circuit (IC) 14 equipped with a precharge function according to the present invention.
Figure 173 shows a case in which the precharge function is provided in the output stage of a 6-bit constant-current output circuit. In Figure 173, a coincidence circuit 1731 performs decoding according to image data D0 to D5 and determines whether

to perform precharging using inputs in an REN terminal and dot clock CLK terminal equipped with a reset function which is based on a horizontal synchronization signal HD. The coincidence circuit 1731 has a memory and retains results of precharging in relation to image data for a few Hs or a few fields (frames). Also, it has capabilities to control precharging by determining whether to perform precharging, based on the retained data. For example, the coincidence circuit 1731 can make settings so as to always perform precharging when the 0th gradation occurs and perform precharging when the 1st gradation occurs consecutively for 6 Hs (six horizontal scanning periods) or more. Also, it can make settings so as to always perform precharging when the 0th or 1st gradation occurs and perform precharging when the 2nd gradation occurs consecutively for 3 Fs (three frame periods) or more.

The output from the coincidence circuit 1731 and output from the counter circuit 701 are ANDed by the AND circuit 703, and consequently a black level voltage Vp is output for a predetermined period. In other cases, the output current from the current output stage 704 described with reference to Figure 68 and the like is applied to the source signal lines 18 (programming current Iw is drawn from the source signal lines 18). The other part of the configuration is the same as or similar to those shown in Figures 70, 75, and the like,

and thus description thereof will be omitted. Incidentally, although the precharge voltage is applied to point A in Figure 173, needless to say, it may be applied to point B (see also Figure 75).

Good results can also be obtained if the duration of application of the precharge voltage PV is varied using the image data applied to the source signal lines 18. For example, the application duration may be increased for the 0th gradation which corresponds to completely black display, and decreased for the 4th gradation. Also, good results can be obtained if the application duration is specified taking into consideration the difference between image data and image data to be applied 1 H later. For example, when writing a current into the source signal lines to put the pixels in black display mode 1 H after writing a current into source signal lines to put the pixels in white display mode, the precharge time should be increased. This is because a weak current is used for black display. Conversely, when writing a current into the source signal lines to put the white pixels in black display mode 1 H after writing a current into source signal lines to put the pixels in black display mode, the precharge time should be decreased or precharging should be stopped (no precharging should be done). This is because a large current is used for white display.

It is also useful to vary the precharge voltage depending

on the image data to be applied. This is because a weak current is used for black display and a large current is used for white display. Thus, the precharge voltage is raised (in relation to Vdd) in a lower gradation region (when P-channel transistors are used as pixel transistors 11a) and the precharge voltage is lowered in a higher gradation region (when P-channel transistors are used as pixel transistors 11a).

For ease of understanding, description will be given below mainly with reference to Figure 75. Needless to say, however, the items described below also apply to precharge circuits shown in Figures 70 and 175.

When a programming current open terminal (PO terminal) is "0," the switch 1521 is off, disconnecting an IL terminal and IH terminal from the source signal line 18 (an Iout terminal is connected with the source signal line 18). Thus, the programming current Iw does not flow through the source signal line 18.

When the programming current Iw is applied to the source signal line, the PO terminal is "1," keeping the switch 1521 on to pass the programming current Iw through the source signal line 18. "0" is applied to the PO terminal to open the switch 1521 when no pixel row in the display area is selected. The unit transistor 634 constantly draws current from the source signal line 18 based on input data (D0 to D5). This current flows into the source signal line 18 from the Vdd

terminal of the selected pixel 16 via the transistor 11a.
Thus, when no pixel row is selected, there is no path for current
to flow from the pixel 16 to the source signal line 18.   A
period when no pixel row is selected occurs after the time
when an arbitrary pixel row is selected until the time when
the next pixel row is selected.   Incidentally, the period
during which no pixel (pixel row) is selected and there is
no path for current to flow into (flow out into) the source
signal line 18 is referred to as total non-selection period.

In this state, if the IOUT terminal is connected to the
source signal line 18, current flows to activated unit
transistors 634 (actually, what is activated are switches 641
controlled by data from the D0 to D5 terminals).
Consequently, charges in the parasitic capacitance of the
source signal line 18 are discharged, lowering the potential
of the source signal line 18 sharply.   Then, it takes time
for the current normally written into the source signal line
18 to restore the potential of the source signal line 18.

To solve this problem, the present invention applies "0"
to the PO terminal during the total non-selection period to
turn off the switch 1521 in Figure 75, and thereby disconnect
the IOUT terminal from the source signal line 18.
Consequently, no current flows from the source signal line
18 into the unit transistors 634, and thus the potential of
the source signal line 18 does not change during the total

non-selection period.   In this way, by controlling the PO terminal during the total non-selection period and disconnecting current sources from the source signal line 18, it is possible to write current properly.

It is useful to add a (proper precharging) capability to stop precharging when a white display area (area with a certain brightness) (white area) and a black display area (area with brightness below a predetermined level) (black area) coexist in the screen and the ratio of the white area to the black area falls within a certain range because vertical streaks appear in this range.   Conversely, precharging may be done in a range because images may act as noise when they move.   Proper precharging can be implemented easily by counting (calculating) pixel data which correspond to the white area and black area using an arithmetic circuit.

It is also useful to vary precharge control among R, G, and B because emission start voltage and emission brightness of EL elements 15 vary among R, G, and B.   For example, a possible method involves stopping or starting precharging for R when the ratio of a white area with a predetermined brightness to a black area with a predetermined brightness is 1 to 20 or above and stopping or starting precharging for G and B when the ratio of a white area with a predetermined brightness to a black area with a predetermined brightness is 1 to 16 or above.   It has been shown experimentally and analytically

that in an organic EL panel, preferably precharging should be stopped when the ratio of a white area with a predetermined brightness to a black area with a predetermined brightness is 1 to 100 or above (i.e., the black area is at least 100 times larger than the white area). More preferably, precharging should be stopped when the ratio of a white area with a predetermined brightness to a black area with a predetermined brightness is 1 to 200 or above (i.e., the black area is at least 200 times larger than the white area). When the driver transistors 11a of the pixels 16 are P-channel transistors, a voltage close to Vdd should be output, as a precharge voltage, from the source driver circuit (IC) 14 (see Figure 1).

However, as the precharge voltage PV gets closer to Vdd, a higher voltage resistance process is required for semiconductors used in the source driver circuit (IC) 14 (the high voltage resistance, however, is only on the order of 5 V to 10 V, but high voltage resistance in excess of 5 V increases the price of the semiconductor process). Thus, adoption of a 5-volt resistance process makes it possible to use high-resolution, inexpensive processes.

If 5 V is not exceeded when the diode characteristics of the driver transistors 11a in pixels 16 are good and on-state current for white display is established, there is no problem because the 5-volt process can also be used for the source

driver IC 14.   However, a problem arises when the diode
characteristics exceed 5 V.   During precharging, in
particular, since a precharge voltage PV close to the source
voltage Vdd of the transistor 11a must be applied, it is not
possible to produce output from the IC 14.

Figure 92 shows a panel configuration used to solve this
problem.   In Figure 92, a switch circuit 641 is formed on
an array board 71.   The source driver IC 14 outputs an on/off
signal for the switch 641.   The on/off signal is boosted
by the level shifter circuit 693 formed on the array board
71 and turns on and off the switch 641.   Incidentally, the
switch 641 and level shifter circuit 693 are formed
simultaneously or sequentially in a process of forming pixel
transistors.   Of course, an external circuit (IC) may be
formed separately and mounted on the array board 71.

The on/off signal is output from the terminal 761a of
the IC 14 according to the precharge conditions described
earlier (Figure 75, etc.).   Thus, needless to say, the
precharge-voltage application and drive method are also
applicable to the example shown in Figure 92.   The voltage
(signal) outputted from the terminal 761a is as low as 5 V
or less.   The voltage (signal) has its amplitude increased
to the on/off logic level of the switch 641 by the level shifter
circuit 693.

With the above configuration, a power supply voltage

capable of driving the programming current Iw in an operating voltage range is enough for the source driver circuit (IC) 14. The precharge voltage PV poses no problem for an array board 71 with a high operating voltage. Thus, the precharge voltage can be applied sufficiently up to the level of the anode voltage (Vdd).

The switch 1521 in Figure 89 also has a problem of voltage resistance if formed (placed) in the source driver circuit (IC) 14. This is because, for example, if the voltage Vdd of the pixels 16 is higher than the power supply voltage of the IC 14, there is a danger that a voltage high enough to break the IC 14 may be applied to the terminal 761 of the IC 14.

An example which can solve this problem is shown in Figure 91. A switch circuit 641 is formed (placed) on an array board 71. Configuration and specifications and the like of the switch circuit 641 are the same as or similar to those described with reference to Figure 92.

The switch circuit 641 is placed ahead of the output of the IC 14 and in the middle of the source signal line 18. As the switch 641 is turned on, the current Iw used to program the pixels 16 flows into the source driver circuit (IC)14. As the switch 641 is turned off, the source driver circuit (IC)14 is cut off from the source signal line 18. By controlling the switch 641, it is possible to implement the

drive system and the like illustrated in Figure 90.

The voltage (signal) outputted from the terminal 761a is as low as 5 V or less, as in the case of Figure 92. The voltage (signal) has its amplitude increased to the on/off logic level of the switch 641 by the level shifter circuit 693.

With the above configuration, a power supply voltage capable of driving the programming current Iw in an operating voltage range is enough for the source driver circuit (IC) 14. Since the switch 641 also operates on the power supply voltage of the array board 71, neither the switch 641 nor the source driver circuit (IC) 14 is broken even if the voltage Vdd is applied to the source signal line 18 from the pixels 16.

Incidentally, needless to say, both the switch 641 placed (formed) in the middle of the source signal line 18 in the Figure 91 and the switch 641 for application of the precharge voltage PV may be formed (placed) on the array board 71 (examples include configurations shown in Figures 91 and 92).

As described earlier, when the driver transistor 11a and selection transistors (11b and 11c) of the pixel 16 are P-channel transistors as shown in Figure 1, a penetration voltage is generated. This is because potential fluctuations of the gate signal line 17a penetrates to a terminal of the capacitor 19 via G-S capacitance (parasitic

capacitance) of the selection transistors (11b and 11c).
When the P-channel transistor 11b turns off, the voltage is
set to Vgh.   As a result, the terminal voltage of the capacitor
19 shifts slightly to the Vdd side.   Consequently, the gate
(G) terminal voltage of the selection transistor 11a rises
creating a more intense black display.   This results in a
proper black display.

However, although a completely black display can be
achieved in the 0th gradation, it is difficult to display the
1st gradation and the like.   In other cases, a large gradation
jump may occur between the 0th and 1st gradations or black
reproduction may occur in a particular gradation range.
To solve this problem, a configuration in Figure 71 is available.
This configuration is characterized by comprising a function
to pad output current values.   A main purpose of a padder
circuit 711 is to make up for the penetration voltage.   It
can also be used to adjust black levels so that some current
(tens of nA) will flow even if image data is at black level
0.

Basically, Figure 71 is the same as Figure 64 except that
the padder circuit has been added (enclosed by dotted lines
in Figure 71) to the output stage.   In Figure 71, three bits
(K0, K1, and K2) are used as current padding control signals.
The three bits of control signals make it possible to add a
current value 0 to 7 times larger than the current value of

grandchild current sources to output current.

The above is a basic overview of the source driver circuit (IC) 14 according to the present invention. Now, the source driver circuit (IC) 14 according to the present invention will be described in more detail.

The current I (A) passed through the EL element 15 and emission brightness B (nt) have a linear relationship. That is, the current I (A) passed through the EL element 15 is proportional to the emission brightness B (nt). In current driving, each step (gradation step) is provided by current (unit transistor 634 (single-unit)).

Human vision with respect to brightness has square-law characteristics. In other words, quadratic brightness changes are perceived to be linear brightness changes. However, according to the relationship shown in Figure 83, the current I (A) passed through the EL element 15 is proportional to the emission brightness B (nt) both in low brightness and high brightness regions. Thus, if brightness is varied step by step (at intervals of one gradation), brightness changes greatly in each step (loss of shadow detail occurs) in a low gradation part (black area). In a high gradation part (white area), since brightness changes coincide approximately with a linear segment of a quadratic curve, the brightness is perceived to change at equal intervals in each step. Thus, how to display a black display area, in particular,

becomes a problem in current driving (in which each step is provided as an increment of current) (i.e., in a current-driven source driver circuit (IC) 14).

To solve this problem according to the present invention, the slope of output current is decreased in the low gradation region (from gradation 0 (complete black display) to gradation (R1)) and the slope of output current is increased in the high gradation region (from gradation R1 to the highest gradation (R)) as illustrated in Figure 79. That is, a current increment per gradation (in each step) is decreased in the low gradation region and a current increment per gradation (in each step) is increased in the high gradation region. By varying the amount of change in current between the two gradation regions in Figure 79, it is possible to bring gradation characteristics close to a quadratic curve, and thus eliminate loss of shadow detail in the low gradation region. Gradation-current characteristics curves illustrated in Figure 79 and the like are referred to as gamma curves.

Incidentally, although two current slopes--in the low gradation region and high gradation region--are used in the above example, this is not restrictive. Needless to say, three or more slopes may be used. Needless to say, however, the use of two slopes is preferable because it simplifies circuit configuration. Preferably, a gamma circuit is capable of generating five or more slopes.

A technical idea of the present invention lies in the use of two or more values of current increment per gradation step in a current-driven source driver circuit (IC) and the like (basically, the circuit uses current outputs for gradation display. Thus, display panels are not limited to the active-matrix type and include the simple-matrix type).

In EL and other current-driven display panels, display brightness is proportional to the amount of current applied. Thus, the source driver circuit (IC) 14 according to the present invention can adjust the brightness of the display panel easily by adjusting a reference current which provides a basis for a current flowing through one current source (one unit transistor) 634.

In EL display panels, luminous efficiency varies among R, G, and B and color purity deviates from that of the NTSC standard. Thus, to obtain an optimum white balance, it is necessary to optimize ratios among R, G, and B. The optimization is performed by adjusting the RGB reference currents separately. For example, the reference current for R is set to 2 µA, the reference current for G is set to 1.5 µA, and the reference current for B is set to 3.5 µA. Preferably, at least one of the reference currents for different colors can be changed, adjusted, or controlled, as described above.

The source driver circuit (source driver IC) 14 according to the present invention decreases the current mirror factor

of the first-stage current source 631 in Figures 67, 148, etc.
(e.g., the current flowing through the transistor 632b is
reduced to 1/100, i.e., to 10 nA if a reference current is
1 μA) to make it possible to roughly adjust the reference current
from outside and accurately adjust minute current within the
chip. Needless to say, the above items also apply to the
reference current Ib in Figure 147 as well as to the reference
currents Ib and Ic in Figures 157, 158, 159, 160, 161, 163,
164, 165, etc.

Adjustment circuits for reference currents in low
gradation regions and adjustment circuits for reference
currents in high gradation regions are provided to achieve
the gamma curve in Figure 79. Incidentally, Figure 79 shows
a gradation control method generated by a single-point
polygonal gamma circuit. This is intended for ease of
explanation and the present invention is not limited to this.
Needless to say a multi-point polygonal gamma circuit may be
used.

Also, although not shown, adjustment circuits for
reference currents in low gradation regions and adjustment
circuits for reference currents in high gradation regions are
provided separately for R, G, and B so that adjustments can
be made separately for R, G, and B. Of course, adjustment
circuits for reference currents in low gradation regions and
adjustment circuits for reference currents in high gradation

regions may be provided for only two colors if white balance
is adjusted by fixing one color and adjusting the reference
currents for two colors (i.e., R and B if G is fixed).

In the case of current driving, the current I passed
through the EL element and brightness have a linear
relationship as also illustrated in Figure 83. To adjust white
balance through a mixture of R, G, and B, it suffices to adjust
the reference currents for R, G, and B at only one predetermined
brightness. In other words, if the white balance is adjusted
by adjusting the reference currents for R, G, and B at the
predetermined brightness, basically a white balance can be
achieved over the entire range of gradations. Thus, the
present invention is characterized by comprising adjustment
means of adjusting the reference currents for R, G, and B as
well as a single-point polygonal or multi-point polygonal gamma
curve generator circuit (generating means). The above is a
circuit arrangement peculiar to current-controlled EL display
panels rather than liquid crystal display panels circuit.

The gamma curve in Figure 79 causes a problem when used
for liquid crystal display panels. To achieve an RGB white
balance, the gamma curve must have the same breakpoint location
(gradation R1) for R, G, and B. The current driving according
to the present invention can accommodate this problem because
it can make relative positions in the gamma curve equal among
R, G, and B. Also, the ratio between slope in a low gradation

region and slope in a high gradation region must be the same among R, G, and B. The current driving according to the present invention can accommodate this problem because it can make relative positions in the gamma curve equal among R, G, and B.

Thus, the current driving according to the present invention operates on the principle that there is a linear relationship between the current I applied to the pixel 16 and emission brightness of the EL element 15 as illustrated in Figure 83 although the slope differ among R, G, and B. The use of this relationship makes it possible to implement a gamma circuit small in scale without disturbing white balance in each gradation.

The gamma circuit of the present invention increments, for example, 10 nA per gradation in a low gradation region (corresponding to the slope of a gamma curve in the low gradation region). In a high gradation region, it increments 50 nA per gradation (corresponding to the slope of a gamma curve in the high gradation region).

Incidentally, the ratio of the current increment per gradation in the high gradation region to the current increment per gradation in the low gradation region is referred to as a gamma current ratio. According to this example, the gamma current ratio is 50 nA/10 nA = 5. The same gamma current ratio should be used for R, G, and B. In other words, the current

(programming current) flowing through the EL elements 15 is controlled with the gamma current ratio kept the same for R, G, and B.

Figure 80 shows an example of gamma curves. In Figure 80(a), the current increases in large per-gradation increments both in the low and high gradation regions. In Figure 80(b), the current increases in smaller per-gradation increments both in the low and high gradation regions than in Figure 80(a). However, both in Figure 80(a) and Figure 80(b), the gamma current ratio is the same for R, G, and B.

If current is adjusted with the gamma current ratio kept the same for R, G, and B in this way, it becomes easier to configure the circuit. Then it suffices to build, for each of R, G, and B, a constant-current circuit which generates a reference current to be applied to the low gradation part and constant-current circuit which generates a reference current to be applied to the high gradation part and build (place) a regulator which relatively adjusts the current passed through the constant-current circuits.

Figure 77 shows a circuit configuration which varies output current while maintaining a gamma current ratio. A current control circuit 772 varies the current passed through current sources 633L and 633H while maintaining the gamma current ratio between a reference current source 771L for low current regions and reference current source 771H for high

current regions.

Preferably, temperature of the display panel is detected with a temperature detection circuit 781 formed in the IC chip (circuit) 14 as illustrated in Figure 78. This is because organic EL elements for R, G, and B vary in temperature characteristics depending on their material. The temperature detection is performed using a bipolar transistor formed in the temperature detection circuit 781. This is based on the principle that junctions of the bipolar transistor change their state with temperature, causing output current of the bipolar transistor to vary with the temperature. The detected temperature is fed back to a temperature control circuit 782 placed (formed) for each color, to allow the current control circuit 772 to make temperature compensation.

Incidentally, an appropriate gamma ratio is between 3 and 10 (both inclusive). More preferably, the gamma ratio is between 4 and 8 (both inclusive). Preferably, the gamma current ratio, in particular, is between 5 and 7 (both inclusive). The above relations will be referred to as a first relationship.

It is appropriate to set a transition point (gradation R1 in Figure 79) between the low gradation part and high gradation part to between 1/32 and 1/4 of the maximum number K of gradations (both inclusive) (e.g., if the maximum number K of gradations is 64 gradations corresponding to 6-bit data,

the transition point should be set to between the 2nd gradation
(= 64/32) and 16th gradation (= 64/4)). More preferably, the
transition point (gradation R1 in Figure 79) between the low
gradation part and high gradation part is set to between 1/16
and 1/4 of the maximum number K of gradations (both inclusive)
(e.g., if the maximum number K of gradations is 64 gradations
corresponding to 6-bit data, the transition point should be
set to between the 4th gradation (= 64/16) and 16th gradation
(= 64/4)). Still more preferably, it is set to between 1/10
and 1/5 of the maximum number K of gradations (both inclusive)
(incidentally, any fractional part is rounded off. For
example, if the maximum number K of gradations is 64 gradations
corresponding to 6-bit data, the transition point should be
set to between the 6th gradation (= 64/10) and 12th gradation
(= 64/5)). The above relations will be referred to as a second
relationship.

Incidentally, the above description concerns gamma
current ratios between two current regions. However, the
second relationship also applies to gamma current ratios among
three or more current regions (i.e., where there are two or
more breakpoints). That is, the relationship can be applied
to any two of three or more slopes.

By satisfying the first and second relationships, it is
possible to achieve proper image display free of loss of shadow
detail.

Figure 82 shows an example in which a plurality of the current-driven source driver circuits (ICs) 14 according to the present invention are used for one display panel. The present invention assumes that a plurality of the source driver ICs 14 are used. The source driver ICs 14 have a slave/master (S/M) terminal.

When the S/M terminal is set to high, the source driver circuit 14 operates as a master chip and outputs a reference current through a reference current output terminal (not shown). This current flows to the INL and INH terminals (in Figures 73 and 74) of slave ICs 14 (14a and 14c). When the S/M terminal is set to low, the source driver circuit 14 operates as a slave chip and receives a reference current from a master chip through a reference current input terminal (not shown). This current flows to the INL and INH terminals in Figures 73 and 74.

Different reference currents are passed between the reference current input terminal and reference current output terminal for different colors in the two gradation regions: low and high. In the case of RGB three colors, this means 6 (= 3 × 6) kinds of reference current. Incidentally, although two kinds of reference current are used for each color in the above example, this is not restrictive and three or more kinds of reference current may be used for each color.

The current driving according to the present invention allows a breakpoint (gradation R1 and the like) to be changed

as illustrated in Figure 81. In Figure 81(a), the low gradation part and high gradation part are divided by gradation R1 while in Figure 81(b), the low gradation part and high gradation part are divided by gradation R2. In this way, the breakpoint location may be selected from among a plurality of locations.

Specifically, the present invention can achieve a 64-gradation display. The breakpoint (gradation R1) can be set to any of the following: none, 2nd gradation, 4th gradation, 8th gradation, and 16th gradation. Incidentally, the reason why the breakpoint can be the 2nd, 4th, 8th, or 16th gradation is that completely black display corresponds to the 0th gradation. If completely black display corresponds to the 1st gradation, the breakpoint can be the 3rd, 5th, 9th, 17th, or 33rd gradation. In this way, if the breakpoint is set to the n-th gradation (or (n + 1)-th gradation if completely black display corresponds to the 1st gradation) where n is a power of two, circuit configuration is made easier.

Figure 73 is a block diagram showing a current source circuit portion for a low-current region. Figure 74 is a block diagram showing a current source portion for a high-current region and padder current circuit portion. As shown in Figure 73, a reference current INL is applied to the low-current source circuit portion. Basically, this current serves as a unit current, a required number of unit transistors 634 operate according to input data L0 to L4, and the total current flows

as a programming current IwL for the low-current portion.

Also, as shown in Figure 74, a reference current INH is applied to the high-current source circuit portion. Basically, this current serves as a unit current, a required number of unit transistors 634 operate according to input data H0 to L5, and the total current flows as a programming current IwH for the low-current portion.

The same applies to the padder current circuit portion. As shown in Figure 74, a reference current INH is applied to it. Basically, this current serves as a unit current, a required number of unit transistors 634 operate according to input data AK0 to AK2, and the total current flows as a current IwK which corresponds to a padding current.

The programming current Iw flowing to the source signal line 18 is given by Iw = IwH + IwL + IwK.
The ratio of IwH to IwL, i.e., the gamma current ratio should satisfy the first relationship described earlier.

As illustrated in Figures 73 and 74, the on/off switch 641 consists of an inverter 732 and an analog switch 731 which in turn consists of a P-channel transistor and N-channel transistor. This configuration can reduce on-resistance and minimize voltage drops between the unit transistor 634 and the source signal line 18. Needless to say, this also applies to other examples of the present invention.

Now, description will be given of the low-current circuit

portion in Figure 73 and high-current circuit portion in Figure 74. The source driver circuit (IC) 14 according to the present invention consists of 5 bits (L0 to L4) in the low-current circuit portion and 6 bits (H0 to H5) in the high-current circuit portion. Incidentally, the data fed into the circuits from outside consists of 6 bits D0 to D5 (64 gradations for each color). The 6-bit data is converted into 5-bit data (L0 to L4) and 6-bit data (H0 to H5) in the high-current circuit portion, and then the programming current Iw corresponding to image data is applied to the source signal line. That is, the 6-bit input data is converted into 11-bit data (= 5 + 6). This makes it possible to form a high-accuracy gamma curve.

As described above, the 6-bit input data is converted into 11-bit data (= 5 + 6). According to the present invention, the bit count (H) in the high-current region of the circuit is equal to the bit count of input data (D) while the bit count (L) in the low-current region of the circuit is equal to the bit count of input data (D) minus 1. Incidentally, the bit count (L) in the low-current region of the circuit may be the bit count of input data (D) minus 2. This configuration optimizes the gamma curve in the low-current region and gamma curve in the high-current region for image display on the EL display panel.

A control method for circuit control data (L0 to L4) in the low-current region and circuit control data (H0 to H4)

in the high-current region will be described below with reference to Figures 84 and 86.

The present invention is characterized by operation of the unit transistor 634a connected to an L4 terminal in Figure 73. The unit transistor 634a consists of a transistor which serves as a single-unit current source. By turning on and off this transistor, the programming current Iw can be controlled easily (on/off control).

Figure 84 shows signals applied to low-current signal lines (L) and high-current signal lines (H) when the low-current region and high-current region are divided by the 4th gradation. Incidentally, although the 0th to 18th gradations are shown in Figures 84 to 86, actually there are gradations up to the 63rd gradation. In this way, the gradations higher than the 18th gradation are omitted in every drawing. The switch 641 turns on when the appropriate value in the table is "1" to connect the appropriate unit transistor 634 with the source signal line 18 and the switch 641 turns off when the appropriate value in the table is "0."

Referring to Figure 84, in the 0th gradation which corresponds to completely black display, (L0 to L4) = (0, 0, 0, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, all the switches 641 are off and the programming current Iw applied to the source signal line 18 is 0.

In the 1st gradation, (L0 to L4) = (1, 0, 0, 0, 0) and

(H0 to H5) = (0, 0, 0, 0, 0). Thus, one unit transistor 634 in the low-current region is connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

In the 2nd gradation, (L0 to L4) = (0, 1, 0, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, two unit transistors 634 in the low-current region are connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

In the 3rd gradation, (L0 to L4) = (1, 1, 0, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, two switches 641La and 641Lb in the low-current region turn on and three unit transistors 634 are connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

In the 4th gradation, (L0 to L4) = (1, 1, 0, 0, 1) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, three switches 641La, 641Lb, and 641Le in the low-current region turn on and four unit transistors 634 are connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

In the 5th and higher gradations, there is no change in the low-current region, i.e., (L0 to L4) = (1, 1, 0, 0, 1). In the high-current region, however, (H0 to H5) = (1, 0, 0, 0, 0) in the 5th gradation. Thus, a switch 641Ha turns on

and one unit current source 641 in the high-current region is connected to the source signal line 18. In the 6th gradation, (H0 to H5) = (0, 1, 0, 0, 0). Thus, a switch 641Hb turns on and two unit current sources 641 in the high-current region are connected to the source signal line 18. Similarly, in the 7th gradation, (H0 to H5) = (1, 1, 0, 0, 0). Thus, two switches 641Ha and 641Hb turn on and three unit current sources 641 in the high-current region are connected to the source signal line 18. In the 8th gradation, (H0 to H5) = (0, 0, 1, 0, 0). Thus, a switch 641Hc turns on and four unit current sources 641 in the high-current region are connected to the source signal line 18 as illustrated in Figure 84. Subsequently, switches 641 turn on and off in sequence and the programming current Iw is applied to the source signal line 18.

A feature of the above operations is that after the breakpoint, the programming current Iw applied to the high gradation part is composed of the current for the low gradation part plus a current which corresponds to each step (gradation) in the high gradation part. A change point of the low-current region and the high-current region, specifically, in the high-current region, for the programming current Iw, low current IwL is added. Therefore, the reference to "change point" may not be correct. A padding current IwK is also added.

Also, control bits (L) in the low gradation region do

not change after a gradation step (a point or location where current changes, to be exact). At this time, the L4 terminal in Figure 73 is set to "1," the switch 641e turns on, and current flows through the unit transistor 634a.

Thus, in the 4th gradation in Figure 84, four unit transistors (current sources) 634 in the low gradation part are in operation. In the 5th gradation, four unit transistors (current sources) 634 in the low gradation part are in operation and one transistor (current sources) 634 in the high gradation part is in operation. Similarly, in the 6th gradation, four unit transistors (current sources) 634 in the low gradation part are in operation and two transistors (current sources) 634 in the high gradation part are in operation. Thus, in the 5th gradation which corresponds to a breakpoint and in the subsequent gradations, as many current sources 634 as there are gradations (four in this case) in the low gradation region below the breakpoint remain on and current sources 634 in the high gradation region turn on in sequence corresponding to the gradation.

It can be seen that the unit transistor 634a at the terminal L4 in Figure 73 operates effectively. Without this transistor 634a, a unit transistor 634 in the high gradation part would turn on after the 3rd gradation. Thus, the change point does not fall on a power of 2 such as 4, 8, or 16. A power of 2 results when only one signal goes "1."

This makes it easy to judge whether a weighting signal line by 2 is set to "1." Consequently, the hardware scale required for the judgment can be reduced. In other words, IC chip logic circuits can be simplified, making it possible to design an IC with a small chip area (resulting in low costs).

Figure 85 is an explanatory diagram illustrating signals applied to low-current signal lines (L) and high-current signal lines (H) when the low-current region and high-current region are divided by the 8th gradation.

Referring to Figure 85, in the 0th gradation which corresponds to completely black display, (L0 to L4) = (0, 0, 0, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0), as in the case of Figure 84. Thus, all the switches 641 are off and the programming current Iw applied to the source signal line 18 is 0.

Similarly, in the 1st gradation, (L0 to L4) = (1, 0, 0, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, one unit transistor 634 in the low-current region is connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

In the 2nd gradation, (L0 to L4) = (0, 1, 0, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, two unit transistors 634 in the low-current region are connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

In the 3rd gradation, (L0 to L4) = (1, 1, 0, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, two switches 641La and 641Lb in the low-current region turn on and three unit transistors 634 are connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

Similarly, in the 4th gradation, (L0 to L4) = (0, 0, 1, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). In the 5th gradation, (L0 to L4) = (1, 0, 1, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). In the 6th gradation, (L0 to L4) = (0, 1, 1, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0). In the 7th gradation, (L0 to L4) = (1, 1, 1, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0).

The 8th gradation corresponds to a change point (breakpoint location). In the 8th gradation, (L0 to L4) = (1, 1, 1, 0, 1) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, four switches 641La, 641Lb, 641Lc, and 641Le in the low-current region turn on and eight unit transistors 634 are connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18.

In the 8th and higher gradations, there is no change in the low-current region, i.e., (L0 to L4) = (1, 1, 1, 0, 1). In the high-current region, however, (H0 to H5) = (1, 0, 0, 0, 0) in the 9th gradation. Thus, the switch 641Ha turns on and one unit current source 641 in the high-current region

is connected to the source signal line 18.

Similarly, the number of unit transistors 634 in the high-current region increases one by one with increasing gradation steps. Specifically, in the 10th gradation, (H0 to H5) = (0, 1, 0, 0, 0). The switch 641Hb turns on and two unit current sources 641 in the high-current region are connected to the source signal line 18. Similarly, in the 11th gradation, (H0 to H5) = (1, 1, 0, 0, 0). Two switches 641Ha and 641Hb turn on and three unit current sources 641 in the high-current region are connected to the source signal line 18. In the 12th gradation, (H0 to H5) = (0, 0, 1, 0, 0). The switch 641Hc turns on and four unit current sources 641 in the high-current region are connected to the source signal line 18. Subsequently, switches 641 turn on and off in sequence and the programming current Iw is applied to the source signal line 18 as illustrated in Figure 84.

Figure 86 is an explanatory diagram illustrating signals applied to low-current signal lines (L) and high-current signal lines (H) when the low-current region and high-current region are divided by the 16th gradation. Basic operation is the same as those in Figures 84 and 85.

Specifically, referring to Figure 86, in the 0th gradation which corresponds to completely black display, (L0 to L4) = (0, 0, 0, 0, 0) and (H0 to H5) = (0, 0, 0, 0, 0), as in the case of Figure 85. Thus, all the switches 641 are off and

the programming current Iw applied to the source signal line 18 is 0. Similarly, from the first to the 16th gradations, (H0 to H5) = (0, 0, 0, 0, 0) in the high-current region. Thus, one unit transistor 634 in the low-current region is connected to the source signal line 18. No unit current source in the high-current region is connected to the source signal line 18. That is, only L0 to L4 in the low-current region change.

Specifically, (L0 to L4) = (1, 0, 0, 0, 0) in the 1st gradation, (L0 to L4) = (0, 1, 0, 0, 0) in the 2nd gradation, (L0 to L4) = (1, 1, 0, 0, 0) in the 3rd gradation, and (L0 to L4) = (0, 0, 1, 0, 0) in the 2nd gradation. This continues to the 16th gradation. Specifically, (L0 to L4) = (1, 1, 1, 1, 0) in the 15th gradation and (L0 to L4) = (1, 1, 1, 1, 1) in the 16th gradation. In the 16th gradation, only the 5th bit (D4) out of D0 to D5 which represent gradations turns on, and thus it can be determined from the data signal line (D4) that the data D0 to D5 represent the 16th gradation. This reduces the hardware scale required for logic circuits.

The 16th gradation corresponds to a change point (breakpoint location). Rather, it ought to be said that the 17th gradation corresponds to a change point. In the 16th gradation, (L0 to L4) = (1, 1, 1, 1, 1) and (H0 to H5) = (0, 0, 0, 0, 0). Thus, four switches 641La, 641Lb, 641Lc, 641d, and 641Le in the low-current region turn on and 16 unit

transistors 634 are connected to the source signal line 18.
No unit current source in the high-current region is connected
to the source signal line 18.

In the 16th and higher gradations, there is no change
in the low-current region, i.e., (L0 to L4) = (1, 1, 1, 0,
1). In the high-current region, however, (H0 to H5) = (1,
0, 0, 0, 0) in the 17th gradation. Thus, the switch 641Ha
turns on and one unit current source 641 in the high-current
region is connected to the source signal line 18.

Similarly, the number of unit transistors 634 in the
high-current region increases one by one with increasing
gradation steps. Specifically, in the 18th gradation, (H0
to H5) = (0, 1, 0, 0, 0). The switch 641Hb turns on and two
unit current sources 641 in the high-current region are
connected to the source signal line 18. Similarly, in the
19th gradation, (H0 to H5) = (1, 1, 0, 0, 0). Two switches
641Ha and 641Hb turn on and three unit current sources 641
in the high-current region are connected to the source signal
line 18. In the 20th gradation, (H0 to H5) = (0, 0, 1, 0,
0). The switch 641Hc turns on and four unit current sources
641 in the high-current region are connected to the source
signal line 18.

The above method results in extremely easy logic
processing such as turning on (or turning off in an alternative
configuration) current sources (single-unit transistors) 634

equal in number to a power of two or connecting them to the source signal line 18 at the change point (breakpoint location).

For example, if the breakpoint location corresponds to the 4th gradation (4 is a power of two) as illustrated in Figure 84, four current sources (single unit) 634 turn on at this location. Then, current sources (single unit) 634 in the high-current region are added in the subsequent gradations.

On the other hand, if the breakpoint location corresponds to the 8th gradation (8 is a power of two) as illustrated in Figure 85, eight current sources (single unit) 634 turn on at this location. Then, current sources (single unit) 634 in the high-current region are added in the subsequent gradations. The present invention makes it possible to implement a gamma control circuit with a small hardware configuration not only for 64-gradation representation, but also for any gradation representation (including 16-gradation representation with 4,096 colors and 256-gradation representation with 16,700,000 colors).

Incidentally, although in the examples described with reference to Figures 84, 85, and 86, it has been stated that the change point is set to the n-th gradation where n is a power of two, this is true only when completely black display corresponds to the 0th gradation. If completely black display corresponds to the 1st gradation, 1 should be added to n.

What is important in the present invention is to provide a plurality of current regions (low-current region, high-current region, etc.) and be able to judge (process) a change point between the current regions using a small number of signal inputs. For example, one technical idea behind the present invention is that if a power of two is used, only a single signal line needs to be detected, reducing the hardware scale greatly. Also, a current source 634a is added to ease the processing required for that.

In the case of negative logic, the change point can be set to 1, 3, 7, 15, or the like instead of 2, 4, 8, or the like. Also, although it has been stated that the 0th gradation corresponds to completely black display, this is not restrictive. For example, in the case of 64-gradation display, the 63rd gradation may be designated as completely black display and the 0th gradation may be designated as a maximum white display. In that case, the change point can be processed, taking into consideration the reverse direction. Thus, processing may not be based on powers of two.

The change point (breakpoint location) is not limited to a single gamma curve. The circuits according to the present invention allows existence of two or more breakpoint locations. For example, breakpoint locations may be set to the 4th and 16th gradations. Alternatively, breakpoint locations may be set to more than two locations such as the 4th, 16th, and 32nd

gradations.

In the above example, the breakpoint is set to the n-th gradation where n is a power of two, but this is not restrictive. For example, a breakpoint may be set to the gradation given by the sum of 2 and 8 which are powers of two (2 + 8 = 10; i.e., two signal lines are needed for judgment). Alternatively, a breakpoint may be set to the gradation given by the sum of 2, 8, and 16 which are powers of two (2 + 8 + 16 = 28; i.e., three signal lines are needed for judgment). In that case, the hardware scale required for judgment or processing is increased more or less, but is not difficult to deal with in terms of circuit configuration. Also, needless to say, the above items are included in the technical scope of the present invention.

As illustrated in Figure 87, the source driver circuit (IC) 14 according to the present invention consists of three current output circuits 704. They are a high-current-region current output circuit 704a which operates in a high current region, low-current-region current output circuit 704b which operates in low and high current regions, and a low-current-region current output circuit 704b which outputs a padding current.

The high-current-region current output circuit 704a and the current-padding current output circuit 704c operate with a reference current source 771a which outputs high current,

as reference current, while the low-current-region current output circuit 704b operates with a reference current source 771b which outputs low current, as reference current.

As also described earlier, the number of current output circuits 704 is not limited to three: the high-current-region current output circuit 704a, low-current-region current output circuit 704b, and current-padding current output circuit 704c. The source driver circuit (IC) 14 may consists of two current output circuits 704--the high-current-region current output circuit 704a and low-current-region current output circuit 704b--or three or more current output circuits 704. Also, reference current sources 771 may be placed or formed for respective current output circuits 704 or a common reference current source 771 may be provided for all the current output circuits 704.

The current output circuits 704 respond to gradation data, and unit transistors 634 in them operate by drawing current from the source signal line 18. Said and unit transistors 634 operate in sync with a horizontal scanning period (1 H) signal. That is, current is fed based on appropriate gradation data for a period of 1 H (if the unit transistors 634 are N-channel transistors).

On the other hand, the gate driver circuit 12 selects gate signal lines 17a basically one by one in sync with the 1 H signal. That is, in sync with the 1-H signal, the gate

signal line 17a (1) is selected in the first horizontal scanning period, gate signal line 17a(2) is selected in the second horizontal scanning period, gate signal line 17a(3) is selected in the third horizontal scanning period, and gate signal line 17a(4) is selected in the fourth horizontal scanning period.

However, between the time when the first gate signal line 17a is selected and the time when the second gate signal line 17a is selected, there is a period in which no gate signal line 17a is selected (non-selection period; see t1 in Figure 88). A rise period and fall period of the first gate signal line 17a are needed for non-selected period in order to secure an on/off control period for the selection transistor 11d.

If a turn-on voltage is applied to any of the gate signal lines 17a and the transistor 11b and selection transistor 11c of the pixel 16 are on, programming current Iw flows from the Vdd power supply (anode voltage) to the source signal line 18 via the driver transistor 11a. The programming current Iw flows through the unit transistors 634 (for a period of t2 in Figure 88). Incidentally, parasitic capacitance C is present in the source signal line 18 (the parasitic capacitance is caused by capacitance at junctions of the source signal line and gate signal lines).

However, when no gate signal line 17a is selected (non-selection period; t1 in Figure 88), there is no current path on the transistor 11a. Since the unit transistors 634

pass current, electric charges are absorbed from parasitic capacitance on the source signal line 18. This lowers the potential of the source signal line 18 (part A in Figure 88). As the potential of the source signal line 18 lowers, it takes time to write current for the next image data.

To solve this problem, a switch 641a is formed at an output end of the source terminal 761 as illustrated in Figure 89. Also, a switch 641b is formed or placed in the output stage of the current-padding current output circuit 704c.

During the non-selection period t1, a control signal is applied to a control terminal S1 and the switch 641a is turned off. During the selection period t2, the switch 641a is turned on (conducting). The programming current $Iw = IwH + IwL + IwK$ flows when the switch 641a is on. When the switch 641a is turned off, the current Iw does not flow. Thus, as illustrated in Figure 90, the potential falls to the level indicated by A in Figure 88 (no change). Incidentally, the channel width W of the analog switch 731 in the switch 641 should be between 10 and 100 μm (both inclusive). The channel width W of the analog switch must be 10 μm or larger to reduce on-resistance. However, it must be no larger than 100 μm because too large W will increase parasitic capacitance. More preferably, the channel width W is between 15 and 60 μm (both inclusive).

The switch 641b performs control only during low gradation

display. During low gradation display (black display), the gate potential of the pixel 16 transistor 11a must be close to Vdd (thus, during black display, the potential of the source signal line 18 must be close to Vdd). Also, during black display, the programming current Iw is small, and once the potential falls as indicated by A in figure 88, it takes time for the potential to return to normal.

Thus, during low gradation display, non-selection periods t1 must be avoided. In contrast, during high gradation display, since the programming current Iw is large, non-selection periods t1 often do not present a problem. Thus, according to the present invention, when images are written for high gradation display, both switch 641a and switch 641b are kept on even during non-selection periods. Also, the padding current IwK must be shut off to achieve black display to the utmost. When images are written for low gradation display, the switch 641a is kept on and the switch 641b is kept off even during non-selection periods. The switch 641b is controlled via terminal S2.

Incidentally, it is also possible to keep the switch 641a off (non-conducting) and keep the switch 641b on (conducting) for both low gradation display and high gradation display during non-selection periods t1. Off course, both switches 641a and 641b may be kept off (non-conducting) for both low gradation display and high gradation display during

non-selection periods t1. In either case, the switches 641 can be controlled by controlling the control terminals S1 and S2. Incidentally, the control terminals S1 and S2 are controlled via command control.

For example, the control terminal S2 sets a t3 period to logic 0 in such a way as to overlap the non-selection period t1. This control eliminates the condition indicated by A in Figure 88. When the gradation represents black display deeper than a certain level, the control terminal S1 is set to logic 0. Then, the padding current IwK is stopped to create a more intense black display.

In a typical driver IC, protective diodes 1671 are formed near the output (see Figure 167). The protective diodes 1671 are formed to prevent the IC 14 from being broken by static electricity from outside. Generally, the protective diodes 1671 are formed between the output wiring 643 and power supply Vcc or between the output wiring 643 and ground.

The protective diodes 1671 are effective for prevention from electrostatic damage. However, static electricity is regarded as a capacitor (parasitic capacitance) in an equivalent circuit diagram. In current driving, presence of parasitic capacitance at an output terminal 643 makes current writing difficult.

The present invention provides a method of solving this problem. The source driver IC 14 is manufactured with the

protective diodes 1671 formed in the output stage. The
manufactured source driver IC 14 is mounted or placed on an
array board 71 and the output terminals 761 are connected to
the source signal lines 18. After the output terminals 761
are connected to the source signal lines 18, the output wiring
643 is cut at points a and b with laser light 1502 as illustrated
in figure 169(a) to cut off the protective diodes 1671.
Also, as illustrated in figure 169(b), laser light 1502 is
directed at points c and d to cut the wiring. Thus, the
protective diodes 1671 become isolated.

In this way, by cutting off the protective diodes 1671
from the output wiring 643 or isolating the protective diodes
1671, it is possible to prevent the protective diodes 1671
from producing parasitic capacitance. Also, since the
protective diodes 1671 are cut off from the output wiring 643
or isolated after the IC 14 is mounted, there is no problem
of electrostatic damage.

Incidentally, the laser light 1502 is directed at the
back surface of the array board 71 as illustrated in Figure
168. The array board 71, which is made of glass, has optical
transparency. Thus, the laser light 1502 can pass through
the array board 71.

It has been assumed in the above example that one source
driver IC 14 is mounted on the display panel. However, the
present invention is not limited to this arrangement. A

plurality of source driver ICs 14 may be mounted on the display panel. For example, Figure 93 shows an example in which three source driver ICs 14 are mounted on a display panel.

As also described with reference to Figure 82, the source driver IC 14 according to the present invention supports the use of two or more current-driven source driver circuits (ICs) 14. Thus, the source driver IC 14 has a slave/master (S/M) terminal. When the S/M terminal is set to high, the source driver circuit 14 operates as a master chip and outputs a reference current through a reference current output terminal (not shown). Of course the logic of the S/M terminal may be reversed.

Slave/master switching may be done through commands given to the source driver IC 14. The reference current is transmitted via a cascade current connection line 931. When the S/M terminal is set to low, the IC 14 operates as a slave chip and receives a reference current from a master chip through a reference current input terminal (not shown). This current flows to the INL and INH terminals in Figures 73 and 74.

To take an example, the reference current is generated by the current output circuit 704 right at the center of the IC chip 14. The reference current for the master chip is adjusted with an external resistor or an internal step-current electronic regulator before it is applied.

A control circuit (command decoder) and the like are also

formed (placed) in the center of the IC chip 14. The reason why the reference current source is formed in the center of the chip is to minimize the distance to the reference current generator circuits and programming current output terminals 761.

In the configuration in Figure 93, reference current is transmitted from a master chip 14b to two slave chips (14a and 14c). Upon receiving the reference current, the slave chips generate parent, child, and grandchild currents based on the received reference current. Incidentally, the master chip 14b delivers current to the slave chips as current-based delivery between current mirror circuits (see Figure 67). The use of current-based delivery eliminates deviations in reference current among the chips as well as parting lines on the screen.

Figure 94 conceptually illustrates locations of terminals among which reference current is delivered. In the center of the IC chip, reference current signal lines 932 are connected to signal input terminals 941i. The current (or voltage; see Figure 76) applied to the reference current signal lines 932 has been compensated for the temperature characteristics of the EL material. Also, it has been compensated for aging of the EL material.

Based on the current (voltage) applied to the reference current signal lines 932, current sources (631, 632, 633, and

634) are driven in the chip 14. The reference currents produced here are output as reference currents for the slave chips via current mirror circuits. The reference currents for the slave chips are output from terminals 941o. At least one terminal 941o is placed (formed) on each side of the current output circuit 704. In Figure 94 two terminals 941o are placed (formed) on each side. The reference currents are transmitted to the slave chips 14 via cascade signal lines 931a1, 931a2, 931b1, and 931b2. Incidentally, it is also possible to adopt a circuit configuration in which the reference current applied to the slave chip 14a is fed back to the master chip 14b to correct deviations. Problems encountered in modularizing an organic EL display panel includes resistance values of anode wiring 951 and cathode wiring.

In the organic EL display panel, although EL elements 15 require a relatively low drive voltage, a large current flows through the EL elements 15. Thus, it is necessary to increase the size of the anode wiring and cathode wiring which supply current to EL element 15. For example, even in a 2-inch class EL display panel, if polymeric EL material is used, 200-mA or higher current must be passed through the anode wiring 951. To reduce voltage drops in the anode wiring 951, the resistance of the anode wiring 951 must be reduced to 1 Ω or below. However, with an array board 71, on which wiring is formed by thin film vapor deposition, it is difficult to reduce

resistance. Therefore, it is necessary to increase pattern width. However, to transmit a 200-mA current with minimum voltage drop, the wiring must be at least 2 mm wide.

Figure 105 shows a configuration of a conventional EL display panel.
Built-in gate driver circuits 12a and 12b are formed (placed) on both sides of a display screen 50. A source driver circuit 14p (built-in source driver circuit) is formed through the same process as pixel 16 transistors.

Anode wiring 951 is placed on the right of the panel. A Vdd voltage is applied to the anode wiring 951. The width of the anode wiring 951 is 2 mm or more, for example. The anode wiring 951 running along the bottom of the screen branches to the top of the screen. The number of branches is equal to the number of pixel columns. For example, a QCIF panel has 528 (= 176 × RGB) pixel columns. On the other hand, source signal lines 18 come out of the built-in source driver circuit 14p. The source signal lines 18 are run (formed) from top to bottom of the screen. Power supply wirings 1051 of the built-in gate driver circuits 12 are also placed on the left and right of the screen.

Thus, bezel width on the right side of the display panel cannot be reduced. Today, reduction of bezel width is important for display panels used for cell phones and the like. It is also important to provide equal bezel width on the left

and right of the screen. With the configuration in Figure 105, however, it is difficult to reduce bezel width.

To solve this problem, in the display panel according to the present invention, the anode wiring 951 is placed (formed) on the surface of the array behind the source driver IC 14 as illustrated in Figure 106. The source driver circuit (IC) 14 is made of a semiconductor chip and mounted on the array board 71 using COG (chip-on-glass) technology. The anode wiring 951 can be placed (formed) on the source driver IC 14 because under the chip 14 is a 10-μm to 30-μm space perpendicular to the board.

As shown in Figure 105, if the source driver circuit 14p is formed directly on the array board 71, it is difficult to form anode wiring (base anode line, anode voltage line, and trunk anode line) 951 above or below the source driver circuit 14p due to issues of the number of masks, yields and noise.

Also, as illustrated in Figure 106, a common anode line 962 is formed and the base anode line 951 and common anode line 962 are short-circuited by connection anode lines 961. One of the points is that the connection anode lines 961 are formed in the center of the IC chip. The connection anode lines 961 eliminates potential difference between the base anode line 951 and common anode line 962. Another point is that anode wires 952 branch off from the common anode line 962. This configuration eliminates routing of anode wiring

951 such as the one shown in Figure 105, and thus can achieve reduction of bezel width.

If the common anode line 962 is 20 mm long, if wiring width is 150 μm, and if sheet resistance of the wiring is 0.05 Ω/□, the value of resistance is given by 20000 (μm)/150 (μm) × 0.05 Ω = approx. 7 Ω. If both ends of the common anode line 962 are connected to the base anode line 951 by a connection anode line 961c, the common anode line 962 is supplied with power from both sides, and consequently an apparent resistance value is 3.5 Ω (= 7 Ω/2). If this value is converted into a concentrated distribution multiplier, the apparent resistance value of the common anode line 962 is further halved and becomes 2 Ω or less. Even if anode current is 100 mA, a voltage drop in the common anode line 962 is 0.2 V or less. Furthermore, if the common anode line 962 and base anode line 951 are short-circuited by the connection anode line 961b in the center, there is almost no voltage drop.

The present invention is characterized in that the base anode line 951 is formed under the IC 14, that the common anode line 962 is formed, that the common anode line 962 is electrically connected to the base anode line 951 (the connection anode line 961), and that the anode wires 952 branch off from the common anode line 962.

Incidentally, the pixel configuration according to the present invention is described by taking the pixel

configuration in Figure 1 as an example. Therefore, the cathode electrode is described as a solid electrode (electrode common to pixels 16) and the anode is described as being wired. However, depending on the configuration of the driver transistor 11a (N-channel or P-channel) or on pixel configuration, it will be necessary to use a solid electrode as the anode and lay a wire as the cathode. Therefore, the present invention is not limited to laying anode wires. The present invention concerns an anode or cathode which needs to be wired. Thus, if the cathode needs to be laid as a wire, description of the anode herein can be applied to the cathode.

To reduce the resistance of anode wires (the base anode line 951, common anode line 962, connection anode lines 961, anode wires 952), a thick film may be formed by laminating conductive material using an electroless plating, electrolytic plating, or other technique after laying thin-film wiring or before patterning. The use of a thick film increases the cross-sectional area of wiring, and thereby reduces resistance. The above items similarly apply to the cathode. They also apply to the gate signal lines 17 and source signal lines 18.

The provision and use of common anode line 962 which is supplied with power from both sides via the connection anode lines 961 is effective and the formation of the connection anode line 961b (961c) in the center enhances this effect.

Also, the base anode line 951, common anode line 962, and connection anode lines 961 form a loop, which can reduce electric fields produced in the IC 14.

Preferably, the common anode line 962 and base anode line 951 are made of the same metal material and the connection anode lines 961 are also made of the same metal material. Also, these anode lines are implemented using a metal material or construction which forms an array and has a very low resistance value. Generally, they are implemented using the same metal material and construction (SD layer) as the source signal lines 18. The same material cannot be used for the spot where the common anode line 962 and source signal line 18 intersect. Thus, another metal material (the same material and construction as the gate signal lines 17; GE layer) is used at the intersections, which are then electrically insulated with an insulating film. Of course, the anode lines may be constructed by laminating a thin film made of the same material as the source signal lines 18 and a thin film made of the same material as the gate signal lines 17.

Incidentally, although it has been stated that wiring such as anode wiring (cathode wiring) is laid on the back surface of the source driver IC 14 to supply current to EL elements 15, this is not restrictive. For example, the gate driver circuits 12 may be constructed with an IC chip and this IC may be mounted by COG. Then, anode wiring and cathode wiring

are laid (formed) on the back surface of the gate driver IC
12.

Thus, the present invention involves fabricating a driver
IC with a semiconductor chip, mounting the IC directly on a
substrate such as an array board 71, and forming (fabricating)
a power supply or ground pattern such as anode wiring and cathode
wiring in a space on the back of the IC chip for an EL display
apparatus or the like.

The above items will be described in more detail with
reference to other drawings. Figure 95 is an explanatory
diagram illustrating part of a display panel according to the
present invention. In Figure 95, dotted lines indicate a
position where the IC chip 14 will be placed. That is, the
base anode line (anode voltage line, i.e., the anode wiring
before branching) is formed (placed) on the back surface of
the IC chip 14 and front surface of the array board 71. In
this example of the present invention, although it is stated
that the anode wiring 951 before branching is formed on the
back surface of the IC chips (12 and 14), this is only for
ease of explanation. For example, cathode wiring or cathode
film before branching may be formed (placed) instead of the
anode wiring 951 before branching. Besides, power supply
wirings 1051 of the gate driver circuits 12 may be placed or
formed.

The IC chip 14 has its current output (current input)

terminals 741 connected by COG technology with connection terminals 953 formed on the array board 71. The connection terminal 953 is formed on one end of each source signal line 18. The connection terminals 953 are arranged in a staggered manner with alternating 953a and 953b. The connection terminal 953 is formed on one end of the source signal line, and a terminal electrode for checking is formed on the other end.

Although it has been stated that the IC chip according to the present invention is a current-driven driver IC (by which pixels are programmed with current), this is not restrictive. For example, the present invention is also applicable to EL display panels (apparatus) equipped with a voltage-driven driver IC by which pixels are programmed with voltage as shown in Figures 43, 53, etc.

The anode wires 952 (anode wiring after branching) are placed between the connection terminals 953a and 953b. That is, the anode wires 952 branching off from the thick, low-resistance base anode line 951 is formed between the connection terminals 953 and laid along the pixel 16 columns. Thus, the anode wires 952 and source signal lines 18 are formed (placed) in parallel. This configuration (formation) makes it possible to apply the voltage Vdd to each pixel without routing the base anode line 951 to the side of the screen as shown in Figure 105.

Figure 96 further illustrates this more concretely. Figure 96 differs from Figure 95 in that instead of being placed between the connection terminals 953, the anode wires branch off from a common anode line 962 formed separately. The common anode line 962 is connected to the base anode line 951 by connection anode lines 961.

Figure 96 illustrates the back surface of the IC chip 14 as seen through the IC chip 14. The IC chip 14 contains current output circuits 704 which output programming current Iw to output terminals 761. Basically, the output terminals 761 and current output circuits 704 are arranged orderly. In the center of the IC chip 14, there are a circuit which generates basic current for a parent current source and a control circuit. Thus, no output terminal 761 is formed in the center of the IC chip 14. This is because no current output circuit 704 can be formed in the center of the IC chip 14.

According to the present invention, in the high-current-region current output circuit 704a part in Figure 96, any output terminals 761 are not provided with the IC chip, because there is no output circuit. Incidentally, it is often the case that although a control circuit is formed, no output circuit is formed in the center of an IC chip such as a source driver. In view of this, the present invention does not form (place) any output terminal 761 in the center of the IC chip 14. Of course, it is not the case when forming (placing) output

terminals 761 in the center of the IC chip 14.

According to the present invention, connection anode lines 961 are formed in the center of the IC chip 14. Needless to say, however, the connection anode lines 961 are formed on a surface of the array board 71. The width of the connection anode lines 961 is between 50 and 1000 μm (both inclusive). Also, the resistance (the maximum resistance) with respect to the length should be 100 Ω or less.

The base anode line 951 and common anode line 962 should be short-circuited by the connection anode lines 961 to minimize voltage drops caused by current flowing through the common anode line 962. That is, the connection anode lines 961, which are a component of the present invention, take advantage of the absence of output circuits in the center of the IC chip. By removing output terminals 761 conventionally formed as dummy pads in the center of the IC chip, the present invention prevents electrical effects which would be caused if the dummy pads contact the connection anode lines 961.

However, if the dummy pads are electrically insulated from a base substrate of the IC chip (ground of the chip) or other structure, there is no problem at all even if the dummy pads contact the connection anode lines 961. Thus, needless to say, the dummy pads may also be formed in the center of the IC chip.

More specifically, the connection anode lines 961 and

common anode line 962 are formed (placed) as shown in figure 99. To begin with, a connection anode line 961 has a thick part (961a) and thin part (961b). The thick part (961a) is intended to reduce resistance value. The thin part (961b) is used to form a connection anode line 961b between output terminals 963 and connect it to the common anode line 962.

The base anode line 951 and common anode line 962 are short-circuited not only via the central connection anode line 961b, but also via the right and left connection anode lines 961c. That is, the common anode line 962 and base anode line 951 are short-circuited by three connection anode lines 961. With this configuration, the common anode line 962 are less prone to voltage drops even if a large current flows through the common anode line 962. This is because the IC chip 14 is normally 2 mm or more in width, making it possible to increase the line width (decrease the impedance) of the base anode line 951 formed under the IC 14. Consequently, the low-impedance base anode line 951 and common anode line 962 are shorted by the connection anode lines 961 at a few locations, reducing voltage drops in the common anode line 962.

The voltage drops in the common anode line 962 can be reduced in this way, because the base anode line 951 can be placed (formed) under the IC chip 14, the connection anode lines 961c can be placed (formed) on left and right of the IC chip 14, and the connection anode line 961b can be placed

(formed) in the center of the IC chip 14.

Also, in Figure 99, the base anode line 951 and a cathode power line (base cathode line) 991 are laminated with an insulating film 102 placed between them. The laminate constitutes a capacitor. This architecture is referred to as an anode capacitor architecture. This capacitor functions as a power path capacitor. Thus, sharp current changes in the base anode line 951 can be absorbed. If the display area of an EL display apparatus is S square millimeters and the capacitance of a capacitor is C (pF), preferably the capacitance of the capacitor satisfies $M/200 \leq C \leq M/10$ or less. More preferably, it satisfies $M/100 \leq C \leq M/20$ or less. A small C makes it difficult to absorb current changes, but too large C makes the formation area of the capacitor too large and is not practical.

Incidentally, it has been stated in the example in Figure 99 and the like that the base anode line 951 is placed (formed) under the IC chip 14, and needless to say, this also applies to the cathode line. Also, in Figure 99, the base anode line 951 may be replaced with the base cathode line 991. A technical idea of the present invention lies in constructing a driver from a semiconductor chip, mounting the semiconductor chip on an array board 71 or a flexible board, and placing (forming) wiring on the back surface of the semiconductor chip to supply power or ground potential (current) to EL elements 15, etc.

Thus, the semiconductor chip may be not only a source driver IC 14, but also a gate driver circuit 12 or power supply IC. Also, the technical idea of the present invention includes mounting a semiconductor chip on a flexible board and laying (forming) a power supply or ground pattern for EL elements 15 or the like in a space on the flexible board and on the back of the semiconductor chip. Of course, both source driver IC 14 and gate driver IC 12 may be constructed of semiconductor chips and mounted on the array board 71 by COG. Then, the power supply or ground pattern may be formed on the back surface of the chips. Also, although it has been stated that the power supply or ground pattern is intended for the EL elements 15, this is not restrictive and the power supply may be intended for the source driver circuit 4 or gate driver circuit 12. Besides, the technical idea of the present invention applies not only to EL display apparatus, but also to liquid crystal display apparatus. It is also applicable to FED, PDP, and other display panels. The above items are also true to other examples of the present invention.

Figure 97 shows another example of the present invention. Figure 97 differs from Figures 95, 96, and 99 mainly in that in Figure 97, a large number of thin connection anode lines 961d branch off from the base anode line 951, short-circuiting to the common anode line 962 whereas in Figure 95, the anode wires 952 are placed between the connection terminals 953.

Also, the thin connection anode lines 961d and source signal lines 18 connected with the connection terminals 953 are laminated with an insulating film 102 placed between them.

The anode lines 961d are connected with the base anode line 951 in contact holes 971a while the anode wires 952 are connected with the common anode line 962 in contact holes 971b. In other respects (the connection anode lines 961a, 961b, 961c and anode capacitor, etc.), Figure 97 is similar to Figures 96 and 99, and thus description thereof will be omitted.

Figure 98 shows a sectional view taken along line a-a' in Figure 99. In Figure 98(a), a source signal line 18 and connection anode line 961d of approximately the same width are laminated with an insulating film 102a placed between them. Preferably, the thickness of the insulating film 102a is between 500 and 3000 Angstrom (Å) both inclusive. More preferably, it is between 800 and 2000 Angstrom (Å) both inclusive. Small film thickness is not desirable because it will increase parasitic capacitance in the connection anode line 961d and source signal line 18 and tend to cause a short circuit between the connection anode line 961d and source signal line 18. On the other hand, thick film thickness will cause insulating-film formation to take time, resulting in long manufacturing time and high cost. Also, wiring on the upper side becomes difficult.

Possible materials for the insulating film 102 include,

for example, organic materials such as polyvinyl alcohol (PVA) resin, epoxy resin, polypropylene resin, phenol resin, acrylic resin, polyimide resin as well as inorganic materials such as SiO2 and SiNx. Needless to say, Al23, Ta2O3, and the like are also included in the possible materials. Also, as illustrated in Figure 98(a), an insulating film 102b is formed in the outermost layer to protect the wiring 961 and the like from corrosion and mechanical damage.

In Figure 98(b), a connection anode line 961d thinner than a source signal line 18 is placed on top of the source signal line 18 with an insulating film 102a placed between them. This configuration prevents steps in the source signal line 18 from causing a short-circuit between the source signal line 18 and connection anode line 961d. In the configuration shown in Figure 98(b), preferably the width of the connection anode line 961d is thinner than that of the source signal line 18 by 0.5 μm or more. More preferably, the connection anode line 961d is thinner than the source signal line 18 by 0.8 μm or more.

Although it has been stated with reference to Figure 98(b) that the connection anode line 961d thinner than the source signal line 18 is placed on top of the source signal line 18 with an insulating film 102a placed between them, it is also possible to place a source signal line 18 thinner than a connection anode line 961d on top of the connection anode line

961d with an insulating film 102a placed between them as illustrated in Figure 98(c). Other items are the same as in other examples, and thus description thereof will be omitted.

Figure 100 shows a sectional view of an IC chip 14. Basically, this configuration is based on the configuration in Figure 99, but it is similarly or analogously applicable to Figures 96, 97, etc.

Figure 100(b) shows a sectional view taken along line A-A' in Figure 99. As can be seen from Figure 100(b), no output pad 761 is formed (placed) in the center of the IC chip 14. The output pads are connected with the source signal lines 18 of the display panel. A bump is formed on the output pads 761 by a plating technique or ball bonding technique. The bump should be 10 to 40 µm high (both inclusive). Of course, it goes without saying that the bump may be formed by a gold plating technique (electrolytic or electroless).

The bumps and the source signal lines 18 are connected electrically via a conductive bonding layer (not shown). The conductive bonding layer is made of an epoxy or phenolic base resin mixed with flakes of silver (Ag), gold (Au), nickel (Ni), carbon (C), tin oxide (SnO2), and the like, or made of an ultraviolet curing resin. The conductive bonding layer (bonding resin) 1001 is formed on the bump by a transfer or other technique. Also, the bumps and the source signal lines 18 are bonded by thermocompression using an ACF resin 1001.

Incidentally, the techniques for connecting the bumps
or output pads 761 with the source signal lines 18 are not
limited to those described above. Besides, a film carrier
technique may be used instead of mounting the IC 14 on the
array board. Also, polyimide films or the like may be used
for connection with the source signal lines 18. Figure 100(a)
is a sectional view of a part where a source signal line 18
and the common anode line 962 overlap (see Figure 98).

Anode wires 952 branch off from the common anode line
962. There are 528 (= 176 × RGB) anode wires 952 in a QCIF
panel. The voltage Vdd (anode voltage) illustrated in Figure
1 and the like is supplied via the anode wires 952. A current
of up to 200 μA flows through one anode wire 952 if the EL
elements 15 are made of low molecular weight-material.
Therefore, a current of approximately 100 mA (200 μA × 528)
flows through the common anode line 962.

Thus, to maintain voltage drops in the common anode line
962 at 0.2 (V) or below, the maximum resistance value of paths
through which the current flows must be maintained at or below
2 Ω (assuming that a current of 100 mA flows). According to
the present invention, since the connection anode lines 961
are formed at three locations as shown in Figure 99, the
resistance value of the common anode line 962 can easily be
minimized in design in terms of a concentrated distribution
circuit. If a large number of connection anode lines 961d

are formed as shown in Figure 97, voltage drops in the common anode line 962 can almost be eliminated.

A problem is the effect of parasitic capacitance (referred to as common anode parasitic capacitance) in portions where the common anode line 962 and source signal lines 18 overlap. Basically, in current driving, presence of parasitic capacitance in source signal lines 18 makes it difficult to write black display current into the source signal lines 18. Thus, parasitic capacitance needs to be minimized.

The common anode parasitic capacitance must not be larger than 1/10 of parasitic capacitance (referred to as display parasitic capacitance) generated by one source signal line 18 in a display area. For example, if the display parasitic capacitance is 10 (pF), the anode parasitic capacitance must be 1 (pF) or less. More preferably, the anode parasitic capacitance is not larger than 1/20 of the display parasitic capacitance. If the display parasitic capacitance is 10 (pF), the anode parasitic capacitance must be 0.5 (pF) or less. The line width (M in Figure 103) of the common anode line 962 and the film thickness of the insulating film 102 (see Figure 101) are determined by taking this point into consideration.

The base anode line 951 is formed (placed) under the IC chip 14. Needless to say, its line width should be as thick as possible to reduce resistance. Besides, preferably the base anode line 951 is provided with a light shielding function.

An explanatory diagram is shown in Figure 102. Needless to say, if the base anode line 951 is formed of a metal material to a required film thickness, it will have a light shielding function. If the base anode line 951 cannot be made thick enough or is made of transparent material such as ITO, light-absorbing film or light-reflecting film is stacked in a single or multiple layers under the IC chip 14 and on the base anode line 951 (basically, on the surface of the array board 71). The light-shielding film (base anode line 951) in Figure 102 does not need to shield light perfectly. It may have openings. Also, it may have diffraction effect or scattering effect. Also, light-shielding film consisting of multilayer optical interference film may be formed or placed by stacking on the base anode line 951.

Of course, a reflector plate (sheet) or light-absorbing plate (sheet) made of a metal foil, plate, or sheet may be placed, inserted or formed in the space between the array board 71 and IC chip 14. Needless to say, it is also possible to place, insert or form a reflector plate (sheet) or light-absorbing plate (sheet) made of a foil, plate or sheet of organic or inorganic material rather than a metal foil. Alternatively, light-absorbing material or light-reflecting material in a gel or liquid state may be inserted or formed in the space between the array board 71 and IC chip 14. Preferably, light-absorbing material or light-reflecting

material in the gel or liquid state are solidified by heating
or by exposure to light.   Incidentally, it is assumed for ease
of explanation that the base anode line 951 is made of a
light-shielding film (light-reflecting film).

As shown in Figure 102, the base anode line 951 is formed
on the surface of the array board 71 (not limited to the surface).
The idea of a light-shielding film or light-reflecting film
can be satisfied if light does not reach the rear surface of
the IC chip 14. Thus, needless to say, the base anode line
951 and the like may be formed on an inner surface or inner
layer of the array board 71. Alternatively, the base anode
line 951 (an arrangement or structure which functions as a
reflecting film or light-shielding film) may be formed on the
rear surface of the array board 71 as long as it can prevent
or reduce entrance of light into the IC 14.

Although it has been stated with reference to Figure 102
and the like that the light-shielding film and the like are
formed on the array board 71, this is not restrictive and the
light-shielding film and the like may be formed directly on
the rear surface of the IC chip 14. In that case, an insulating
film 102 (not shown) is formed on the rear surface of the IC
chip 14 and the light-shielding film, reflecting film, or the
like is formed on the insulating film. When forming the source
driver circuit 14 directly on the array board 71 (driver
construction by low-temperature polysilicon technology,

high-temperature polysilicon technology, solid-phase growth
technology, or amorphous silicon technology), the source
driver circuit 14 can be formed (placed) on the light-shielding
film, light-absorbing film, or reflecting film which is formed
on the array board 71.

A large number of transistor elements, such as current
sources 634, which pass minute current are formed on the IC
chip 14 (circuit forming section 1021 in Figure 102). When
light enters transistor elements (such as unit transistors
634) which pass minute current, a photoconduction phenomenon
and the like occur, making values of output current
(programming current Iw), parent current, child current, etc.
abnormal (causing variations, and the like). In the case of
organic EL or other self-luminous elements, in particular,
light produced by the EL elements 15 is reflected diffusely
within the array board 71, causing intense light to be radiated
from places other than the display screen 50. The radiated
light, upon entering the circuit forming section 1021 of the
IC chip 14, causes the photoconduction phenomenon. Thus,
measures against the photoconduction phenomenon are measures
against a problem peculiar to EL display devices.

To deal with this problem, the present invention
constructs the base anode line 951 on the array board 71 and
uses it as a light-shielding film. The formation area of the
base anode line 951 covers the circuit forming section 1021

as illustrated in Figure 102. By forming the light-shielding film (base anode line 951) in this way, it is possible to prevent the photoconduction phenomenon completely. As the screen is refreshed, current flows through EL power lines such as the base anode line 951, in particular, causing some changes to their potential. However, since the potential changes little by little every horizontal scanning period, it can be regarded as ground potential (meaning that there is virtually no change in the potential). Thus, the base anode line 951 or base cathode line performs not only a light-shielding function, but also an electric shielding function.

In the case of organic EL or other self-luminous elements, light produced by the EL elements 15 is reflected diffusely within the array board 71, causing intense light to be radiated from places other than the display screen 50. To prevent or reduce the diffusely reflected light, light-absorbing films 1011 are formed in ineffective areas which do not pass light effective for image display as illustrated in Figure 101 (on the other hand, effective areas are the display screen 50 and areas around it). The light-absorbing films are formed on an outer surface of a sealing lid 85 (light-absorbing film 1011a), inner surface of the sealing lid 85 (light-absorbing film 1011c), side face of the board 70 (light-absorbing film 1011d), area on the board other than the image display area (light-absorbing film 1011b), etc. Incidentally, instead of

light-absorbing films, light-absorbing sheets or
light-absorbing walls may be installed. Besides, the concept
of light absorption also includes schemes or structures which
diverge light by scattering it. In a broader sense, it also
includes schemes or structures which confine light through
reflection.

Possible materials for light-absorbing films include,
for example, organic material such as acrylic resin containing
carbon, organic resin with a black pigment dispersed in it,
and gelatin or casein colored with a black acidic dye as with
a color filter. Besides, they also include a fluorine-based
pigment which singly develops a black color as well as green
and red pigments which develop a black color when mixed.
Furthermore, they also include $PrMnO_3$ film formed by sputtering,
phthalocyanine film formed by plasma polymerization, etc.

All the above materials develop black colors, but
materials which develop a color complementary to the color
developed by display elements may also be used for the
light-absorbing films. For example, light-absorbing
materials for color filters can be used by modifying them so
as to provide desired light-absorbing characteristics.
Basically, natural resin colored by dyes may be used as is
the case with the black light-absorbing materials described
above. It is also possible to use plastics in which dyes are
dispersed. In that case, an available range of pigments is

wider than in the case of black pigments and includes azo dyes, anthraquinone dyes, phthalocyanine dyes, and triphenylmethane dyes. An appropriate one of them or a combination of two or more of them may be used.

Besides, metal materials may also be used for the light-absorbing films. Possible materials include, for example, hexavalent chromium. Hexavalent chromium is black in color and functions as a light-absorbing film. Besides, light-scattering materials such as opal glass and titanium oxide are also available. By scattering light, it is often possible to absorb light as a result.

Incidentally, the sealing lid 85 is bonded to the array board 71 using a sealing resin 1031 containing resin beads 1012 from 4 μm to 15 μm (both inclusive) in diameter. The sealing lid 85 is placed without applying pressure and fixed.

The example illustrated in Figure 99 involves forming (placing) the common anode line 962 near the IC chip 14, but this is not restrictive. For example, the common anode line 962 may be formed near the display screen 50 as illustrated in Figure 103. Rather, this is preferable because this will reduce parts where the source signal lines 18 and anode wires 952 are placed at short distances in parallel with each other. If the source signal lines 18 and anode wires 952 are placed at short distances in parallel with each other, parasitic

capacitance will be produced between them. This problem can be solved if the common anode line 962 is placed near the display screen 50 as illustrated in Figure 103. Preferably, the distance K (see Figure 103) from the display screen 50 to the common anode line 962 is 1 mm or less.

Preferably, the common anode line 962 is made of the same metal material as the source signal lines 18 to minimize its resistance. According to the present invention, it is made of metal material (SD metal) such as thin Cu film, thin Al film, Ti/Al/Ti laminate, alloy, or amalgam. Thus, this material is replaced by the same metal material (GE metal) as the gate signal lines 17 at intersections of the source signal lines 18 and common anode line 962 to prevent short circuits. The gate signal lines are made of metal material, namely a Mo/W laminate.

Generally, the sheet resistance of gate signal lines 17 is higher than the sheet resistance of source signal lines 18. This is common to liquid crystal display apparatus. However, in organic EL display panels of a current-driving type, the current flowing through source signal lines 18 is as weak as 1 to 5 μA. Thus, even if the source signal lines 18 have a high resistance, almost no voltage drop occurs, and thus proper image display can be achieved. In liquid crystal display apparatus, image data is written into the source signal lines 18 by way of voltage. Thus, if the source signal lines

18 have a high resistance value, it is not possible to write images in one horizontal scanning period.

With the current driving according to the present invention, however, a high resistance value (i.e., a high sheet resistance value) of the source signal lines 18 does not pose a problem. Therefore, the sheet resistance of the source signal lines 18 may be higher than the sheet resistance of the gate signal lines 17. Thus, in the EL display panel of the present invention, the source signal lines 18 may be made (formed) of GE metal and the gate signal lines 17 may be made (formed) of SD metal as illustrated in Figure 104 (contrary to liquid crystal display panels). In a broader sense, in the EL display panel of a current-driving type, the wiring resistance of the source signal lines 18 is higher than the wiring resistance of the gate signal lines 17.

A configuration in Figure 107 contains power wiring 1051 for driving gate driver circuits 12 in addition to the configurations in Figures 99 and 103. The power wiring 1051 is routed from the right edge of the display screen 50 through the bottom side to the left edge of the display screen 50. That is, gate driver circuits 12a and 12b have a common power supply.

Preferably, however, the gate driver circuit 12a which selects the gate signal line 17a (which controls the selection transistors 11b and 11c) and gate driver circuit 12b which

selects the gate signal line 17b (which controls the transistor 11d and current flowing through the EL element 15) have different power supply voltages. In particular, it is preferable that the amplitude (difference between turn-on voltage and turn-off voltage) of the gate signal line 17a is small. This is because the smaller the amplitude of the gate signal line 17a, the smaller the penetration voltage to the capacitor 19 in the pixel 16 (see Figure 1, etc.) On the other hand, the amplitude of the gate signal line 17b cannot be decreased because the gate signal line 17b must control the EL element 15.

Thus, as illustrated in Figure 108, applied voltages of the gate driver circuit 12a are Vha (turn-off voltage for the gate signal line 17a) and Vla (turn-on voltage for the gate signal line 17a) while applied voltages of the gate driver circuit 12a are Vhb (turn-off voltage for the gate signal line 17b) and Vla (turn-on voltage for the gate signal line 17b). A relationship Vla < Vlb should be satisfied. Incidentally, Vha and Vhb may be approximately equal.

Normally, N-channel transistors and P-channel transistors are used for the gate driver circuits 12, but preferably, only P-channel transistors are used. This is because it will reduce the number of masks used in fabrication of arrays, increase production yields, and improve throughput. Thus, as illustrated in Figures 1, 2, etc., P-channel

transistors should be used for the pixels 16 as well as for the gate driver circuits 12. Ten masks are required if N-channel transistors and P-channel transistors are used for a gate driver circuit, but five masks are required if only P-channel transistors are used.

However, if only P-channel transistors are used for the gate driver circuits 12 and the like, no level shifter circuit can be formed on the array board 71. This is because level shifter circuits employ N-channel transistors and P-channel transistors.

To solve this problem, the present invention incorporates level shifter circuit functions into a power supply IC 1091. Figure 109 shows an example of this. The power supply IC 1091 generates the drive voltage of the gate driver circuits 12, anode voltage and cathode voltage of the EL elements 15, and drive voltage of the source driver circuit 14.

To generate the anode and cathode voltages of the EL elements 15 of the gate driver circuits 12, the power supply IC 1091 needs to employ high voltage semiconductor processes. Such voltage resistance allows a level shift to signal voltage of the gate driver circuits 12. Also, as illustrated in Figure 205, level shifter circuits 2041 may be formed in the source driver IC 14. The level shifter circuits 2041 may be formed on left and right sides of the source driver IC 14. When using more than one source driver IC 14 as shown in Figure 205, one

of the level shifter circuits 2041 in each source driver IC 14 is used.

In Figure 205, a level shifter circuit 2041a in a source driver IC 14a is used. Gate control data is boosted by the level shifter circuit 2041a to become a gate driver control signal 2043a and controls the gate driver circuit 12a. Also, a level shifter circuit 2041b in a source driver IC 14b is used. Gate control data is boosted by the level shifter circuit 2041b to become a gate driver control signal 2043b and controls the gate driver circuit 12b.

The configurations in Figure 109 is used to perform level shifting and drive the gate driver circuits 12. Input data (image data, commands, and control data) 992 are fed into the source driver IC 14. The input data also contains control data of the gate driver circuit 12. The source driver IC 14 has a voltage resistance (operating voltage) of 5 (V). On the other hand, the gate driver circuits 12 have an operating voltage of 15 (V). The signal outputted from the source driver circuit 14 to the gate driver circuits 12 must be level-shifted from 5 (V) to 15 (V). The level shifting is performed by the power supply circuit (IC) 1091. In Figure 109, a data signal for use to control the gate driver circuits 12 is designated as a power supply IC control signal 1092.

Upon receiving the data signal 1092 for use to control the gate driver circuits 12, the power supply circuit 1091

level-shifts it with a built-in level shifter circuit and outputs the resulting signal as a gate driver circuit control signal 1093 to control the gate driver circuits 12.

Now description will be given of the gate driver circuits 12 according to the present invention which are contained in the array board 71 and employ only P-channel transistors. As described earlier, by employing only P-channel transistors for the pixels 16 and gate driver circuits 12 (i.e., the transistors formed on the array board 71 are only P-channel transistors, meaning that no N-channel transistor is used), it is possible to reduce the number of masks used in fabrication of arrays, increase production yields, and improve throughput. Also, since it is possible to focus on improving performance of only P-channel transistors, characteristics can be improved easily as a result. For example, it is easier to lower threshold voltage (Vt) (bring it closer to 0 (V)) and reduce variations in the Vt than in the case of CMOS structures (an arrangement using P-channel and N-channel transistors).

To take an example, according to the present invention, one gate driver circuit 12 each is placed on a phase basis (shift registors), formed or constructed on the left and right of the display screen 50 as illustrated in Figure 106. Although it is assumed that gate driver circuits 12 and the like (including pixel 16 transistors) are formed or constructed by low-temperature polysilicon technology at a process

temperature of 450 degrees (centigrade) or lower, this is not restrictive. It is also possible to use transistors produced by high-temperature polysilicon technology at a process temperature of 450 degrees (centigrade) or higher, or transistors made of CGS semiconductor films produced by solid-phase growth. Besides, organic transistors are also available. Alternatively, transistors may be formed or constructed by amorphous silicon technology.

One of the gate driver circuits 12 is a selection-side gate driver circuit 12a. It controls the pixel transistors 11 by applying turn-on voltage or turn-off voltage to the gate signal lines 17a. The other gate driver circuit 12b turns on and off the current passed through the EL elements 15.

Although the examples of the present invention is described by mainly taking the pixel configuration in Figure 1 as an example, this is not restrictive. Needless to say, the present invention is also applicable to other pixel configurations shown in Figures 50, 51, 54, etc. Also, the configuration or drive system of the gate driver circuits 12 according to the present invention produce more characteristic effects if combined with the display panel, display apparatus, or information display apparatus according to the present invention. Needless to say, however, the gate driver circuits 12 can also produce characteristic effects even when other configurations are employed.

Incidentally, the configuration or layout of the gate driver circuit 12 described below is not limited to self-luminous devices such as organic EL display panels. It can also be used for liquid crystal display panels, electromagnetic display panels, etc. For example, liquid crystal display panels may employ the configuration or arrangement of the gate driver circuit 12 according to the present invention to control pixels' selection switching elements. If two gate driver circuits 12 are used, one of them may be used to select pixels' switching elements and the other may be connected to one terminal of a retention capacitance in each pixel. This scheme is referred to as independent CC driving. Needless to say, the configurations described with reference to Figures 111, 113, etc. can also be used not only for the gate driver circuits 12, but also for the shift register circuits and the like, of the source driver circuit 14.

Preferably, the gate driver circuit 12 described here is implemented or adopted as the gate driver circuits 12 described earlier with reference to Figures 6, 13, 16, 20, 22, 24, 26, 27, 28, 29, 34, 37, 40, 41, 48, 82, 91, 92, 93, 103, 104, 105, 106, 107, 108, 109, 176, 181, 187, 188, 208, etc.

Figure 111 is a block diagram of the gate driver circuit 12 according to the present invention. Although only four

stages are illustrated for ease of explanation, basically there
are formed or placed as many unit gate output circuits 1111
as there are gate signal lines 17.

As illustrated in Figure 111, the gate driver circuits
12 (12a and 12b) according to the present invention comprise
signal terminals: four clock terminals (SCK0, SCK1, SCK2, and
SCK3), one start terminal (data signal (SSTA)), and two
inverting terminals (DIRA and DIRB which apply signals 180
degrees out of phase with each other) which turn a shift
direction upside down. They also comprise power supply
terminals, including an L power supply terminal (VBB) and H
power supply terminal (Vd).

Since only P-channel transistors are used for the gate
driver circuits 12 here, no level shifter circuit (circuit
used to convert a low voltage logic signal into a high voltage
logic signal) can be incorporated into the gate driver circuits.
Thus, the level shifter circuit is placed or formed in the
power supply circuit (IC) 1091 shown in Figure 109 and the
like.

The power supply circuit (IC) 1091 generates voltages
of potentials needed for a turn-on voltage (selection voltage
of pixel 16 transistors) and turn-off voltage (non-selection
voltage of pixel 16 transistors) to be output from the gate
driver circuits 12 to the gate signal lines 17. Consequently,
semiconductor processes for the power supply IC (circuit) 1091

have sufficient voltage resistance. Thus, the logic signals can be level-shifted (LS) conveniently by the power supply IC 1091. For this reason, gate driver circuit 12 control signals outputted from a controller (not shown) are fed into the power supply IC 1091 and level-shifted there before it is fed into the gate driver circuits 12 according to the present invention. Source driver circuit 14 control signals outputted from the controller (not shown) are fed into the source driver circuit 14 and the like according to the present invention directly (there is no need for level shifting).

However, the present invention does not limit all the transistors formed on the array board 71 to P-channel transistors. By using only P-channel transistors for the gate driver circuits 12 as described later with reference to Figures 111 and 113, it is possible to reduce bezel width. In the case of a 2.2-inch QCIF panel, the width of a gate driver circuit 12 can be constructed of 600 μm if a 6-μm rule is adopted. The width will be 700 μm even including power wiring of the supplying gate driver circuit 12. If CMOS (N-channel and P-channel transistors) is used for a similar circuit configuration, the width will be increased to 1.2 mm. Thus, by using only P-channel transistors for the gate driver circuits 12, it is possible to achieve a characteristic effect of bezel width reduction.

Also, if the pixels 16 are constructed of P-channel

transistors, they will match well with the gate driver circuits 12 which employ P-channel transistors. The P-channel transistors (the selection transistors 11b and 11c and transistor 11d in the configuration in Figure 1) turn on when the voltage becomes low. On the other hand, the lower voltage serves as the selection voltage for the gate driver circuits 12 as well. Gate drivers with P-channel achieve good matching if the lower level is used as the selection level as can be seen from a configuration in Figure 113. This is because the lower level cannot be maintained for a long time. On the other hand, the higher voltage can be maintained for a long time.

Also, by using P-channel for the driver transistors (transistor 11a in Figure 1) which supply current to the EL element 15, it is possible to use a solid electrode made of thin metal film as the cathode of the EL elements 15. Also, current can be passed from the anode potential Vdd to the EL elements 15 in the forward direction. In view of the above circumstances, it is preferable that the transistors in the pixels 16 and gate driver circuits 12 are P-channel. Thus, the use of P-channel transistors as the transistors (driver transistors and itching transistors) in the pixels 16 and gate driver circuits 12 according to the present invention is not merely a design matter.

In this sense, the level shifter (LS) circuit may be formed directly on the array board 71. That is, N-channel and

P-channel transistors are used for the level shifter (LS) circuit. A logic signal from a controller (not shown) is boosted by the level shifter circuit formed directly on the array board 71 so that it will match the logic level of the gate driver circuits 12 constructed from a P-channel transistor. The boosted logic voltage is applied to the gate driver circuits 12.

Incidentally, the level shifter circuit may be constructed from a semiconductor chip and mounted on the array board 71 using COG technology or the like. Also, the source driver circuit 14 is constructed basically from a semiconductor chip and mounted on the array board 71 using COG technology, as illustrated in Figure 109 and the like. However, this is not restricted to forming the source driver circuit 14 as a semiconductor chip and the source driver circuit 14 may be formed directly on the array board 71 using polysilicon technology. If P-channel transistors are used as the transistors 11 of pixels 16, programming current flows in the direction from the pixels 16 to the source signal lines 18. Thus, N-channel transistors should be used as the unit current circuits 634 of the source driver circuits (see Figures 73 and 74). That is, the source driver circuits 14 should be configured in such a way as to draw the programming current Iw.

Thus, if the driver transistors 11a of the pixels 16 (in the case of Figure 1) are P-channel transistors, the unit transistors 634 of the source driver circuits 14 must be N-channel transistors to ensure that the source driver circuits 14 will draw the programming current Iw. In order to form a source driver circuit 14 on an array board 71, it is necessary to use both mask (process) for N-channel transistors and mask (process) for P-channel transistors. Conceptually speaking, in the display panel (display apparatus) of the present invention, P-channel transistors are used for the pixels 16 and gate driver circuits 12 while N-channel transistors are used as the transistors of drawing current sources of the source drivers.

Incidentally, for ease of explanation, the pixel configuration in Figure 1 is employed in the example of the present invention. However, the technical idea of the present invention which involves the use of P-channel transistors as selection transistors (transistor 11c in Figure 1) of pixels 16 and for gate driver circuits 12 is not limited to the pixel configuration in Figure 1. Needless to say, for example, it is also applicable to the current-mirror pixel configuration illustrated in Figure 42 in the case of current-driven pixel configuration. Also, it is applicable to two transistors (selection transistor is transistor 11b and driver transistor is transistor 11a) such as those illustrated in Figure 62 in

the case of voltage-driven pixel configuration. Of course, it is also applicable to the gate driver 12 configurations in Figures 111 and 113 and they can be combined to construct an apparatus. Thus, the items described above as well as the items described below are not limited to pixel configuration or the like.

The configuration in which P-channel transistors are used as selection transistors of pixels 16 and for gate driver circuits is not limited to organic EL or other self-luminous devices (display panels or display apparatus). For example, it is also applicable to liquid crystal display panels and FEDs (field emission displays).

The inverting terminals (DIRA and DIRB) apply common signals to all the unit gate output circuits 1111. As can be seen from an equivalent circuit diagram in Figure 113, inverting terminals (DIRA and DIRB) are fed voltage values of opposite polarity. To reverse the scan direction of the shift register, the polarity of the voltage values fed into the inverting terminals (DIRA and DIRB) is reversed.

Incidentally, the circuit configuration in Figure 111 contains four clock signal lines. Four is the optimum number according to the present invention. However, this is not restrictive and the present invention may use less than or more than four clock signal lines.

The clock signals (SCK0, SCK1, SCK2, and SCK3) are fed differently between adjacent unit gate output circuits 1111. For example, in the unit gate output circuit 1111a, OC is fed by the clock terminal SCK0 while RST is fed by the clock terminal SCK2. This is also the case with the unit gate output circuit 1111c. However, in the unit gate output circuit 1111b (the unit gate output circuit in the next stage) adjacent to the unit gate output circuit 1111a, OC is fed by the clock terminal SCK1 while RST is fed by the clock terminal SCK3. In this way, every other unit gate output circuit 1111 is fed by clock terminals in a different manner: OC is fed by SCK0 and RST is fed by SCK2, OC is fed by SCK1 and RST is fed by SCK3 in the next stage, OC is fed by SCK0 and RST is fed by SCK2 in the next stage, and so on.

Figure 113 shows a circuit configuration of the unit gate output circuit 1111, which uses only P-channel transistors. Figure 114 is a timing chart for use to explain the circuit configuration of Figure 113. Figure 112 is a timing chart of multiple stages in Figure 113. Thus, by understanding Figure 113, it is possible to understand overall operation. Rather than being explained in text, the operation can be understood with reference to the timing chart in Figure 114 in conjunction with the equivalent circuit diagram in Figure 113, and thus detailed description of transistor operation will be omitted.

When driver circuits are built solely of P-channel transistors, it is basically difficult to maintain the gate signal lines 17 at an H level (Vd voltage in Figure 113). It is also difficult to maintain them at an L level (VBB voltage in Figure 113) for a long period of time, but they can be kept adequately at the H level for a short period such as during selection of a pixel row. A signal fed to an IN terminal and the SCK clock fed to the RST terminal invert the state of n1 with respect to n2. Although n2 and n4 have potentials of the same polarity, the SCK clock fed to the OC terminal lowers the potential level of n4 further. In contrast, a Q terminal is kept at the L level for the same period (a turn-on voltage is output from the gate signal line 17). A signal outputted to an SQ terminal or the Q terminal is transferred to the unit gate output circuit 711 in the next stage.

In the circuit configuration in Figures 111 and 113, by controlling the IN (INA and INB) terminals and the timings of signal application to clock terminals, it is possible to two modes using the same circuit configuration: a mode in which one gate signal line 17 is selected as shown in Figure 115(a) and a mode in which two gate signal lines 17 are selected as shown in Figure 115(b).

In the selection-side gate driver circuit 12a, Figure 115(a) shows a drive mode in which pixel rows are selected one (51a) at a time (normal driving) shifting on a row-by-row

basis.   Figure 115(b) shows a configuration in which two pixel rows are selected at a time.   This drive mode corresponds to the driving for simultaneous selection of multiple pixel rows (51a and 51b) described with reference to Figures 27 and 28 (configuration in which a dummy pixel row is used).   Two adjacent rows are selected at a time shifting on a row-by-row basis.   According to the drive method in Figure 115(b) in particular, while the pixel row (51a) holds final video, the pixel row 51b is precharged.   This makes the pixel 16 easier to write into.   That is, the present invention can switch between two drive modes by manipulating signals applied to terminals.

Incidentally, although 115(b) shows a mode in which adjacent rows of pixels 16 are selected as shown in Figure 116, it is also possible to select rows of pixels 16 other than adjacent pixel rows (Figure 116 shows an example in which pixel rows three pixel rows apart are selected).   In the configuration shown in Figure 113, pixel rows are controlled in sets of four.   Out of four pixel rows, it is possible to determine whether to select one pixel row or two consecutive pixel rows.   The number of pixel rows in each set is restricted by the number of clocks (SCK), which is four in this case. If eight clocks (SCK) are used, pixel rows can be controlled in sets of eight.

Operation of the selection-side gate driver circuit 12a

is shown in Figure 115. In Figure 115(a), one pixel row is selected at a time and selection position is shifted by one pixel row in sync with a horizontal synchronization signal. In Figure 115(b), two pixel rows are selected at a time and selection position is shifted by one pixel row in sync with a horizontal synchronization signal.

As illustrated in Figure 182, connection anode lines 961 are wired from an anode connection terminal 1821 and the connection anode lines 961 formed on both sides of a source driver IC 14 are connected electrically by means of a switch 2021 formed under the IC 14.

A common anode line 962 is formed or placed on the output side of the source driver IC 14. Anode wires 952 branch off from the common anode line 962. There are 528 (= 176 × RGB) anode wires 952 in a QCIF panel. The voltage Vdd (anode voltage) illustrated in Figure 1 and the like is supplied via the anode wires 952. A current of up to on the order of 200 μA flows through one anode wire 952 if the EL elements 15 are made of low molecular weight-material. Therefore, a current of approximately 100 mA (200 μA × 528) flows through the common anode wire 833.

To reduce voltage drops in the common connection anode lines 961 and anode wires 952, it is recommended to form a common connection anode line 961a on the upper side of the display screen 50, form a common connection anode line 961b

on the lower side of the display screen 50, and short-circuit the anode wires 952 at its top and bottom as illustrated in Figure 183.

It is also preferable to place source driver circuits 14 at the top and bottom of the screen 50 as illustrated in Figure 184. It is also possible to divide the display screen 50 into a display screen 50a and display screen 50b and drive the display screen 50a with a source driver circuit 14a, and the display screen 50b with a source driver circuit 14b as illustrated in Figure 185.

Figure 201 is a block diagram of the power supply circuit according to the present invention. Reference numeral 2012 denotes a control circuit, which controls the midpoint potential of resistances 2015a and 2015b and outputs a gate signal of a transistor 2016. A power supply Vpc is applied to the primary side of a transformer 2011 and primary current is transmitted to the secondary side under on/off control of the transistor 2016. Reference numeral 2013 denotes a rectifying diode and 2014 denotes a smoothing capacitor.

Anode voltage Vdd has its output voltage adjusted to a resistor 2015b. Vss denotes cathode voltage. One of two voltages can be output selectively as the cathode voltage Vss as illustrated in Figure 202. Switch 2021 is used for the selection. In Figure 202, -9 (V) is selected by the switch 2021.

The switch 2021 is operated according to output from a temperature sensor 2022. When panel temperature is low, -9(V) is selected as the voltage Vss. When the panel temperature is equal to or higher than a certain level, -6(V) is selected. This is because EL elements 15 have temperature dependence and terminal voltage of the EL elements 15 becomes higher on a low temperature side. Incidentally, although it has been stated with reference to Figure 202 that one of two voltages is selected as Vss (the cathode voltage), this is not restrictive and the voltage Vss may be selected from three voltages. The above items similarly apply to Vdd.

By allowing a voltage to be selected from a plurality of voltages based on panel temperature as shown in Figure 202, it is possible to reduce power consumption of the panel. This is because the voltage Vss can be lowered when the temperature is equal to or lower than a certain level. Normally, the lower Vss (= -6(V)) can be used. Incidentally, the switch 2021 may be configured as illustrated in Figure 202. A plurality of voltages Vss can be generated easily by using intermediate taps of a transformer 2011 in Figure 202. This similarly applies to the anode voltage Vdd.

Figure 205 is an explanatory diagram illustrating potential setting. The source driver IC 14 is based on GND. The power supply for the source driver IC 14 is Vcc. Vcc may be brought to coincide with the anode voltage (Vdd). According

to the present invention, Vcc < Vdd from the viewpoint of power consumption.

The turn-off voltage Vgh of the gate driver 12 is set to equal to or higher than the voltage Vdd. Preferably, Vdd + 0.5 (V) < Vgh < Vdd + 2.5 (V) is satisfied. The turn-on voltage Vgl may be brought to coincide with Vss, but preferably Vss (V) < Vgl < -0.5 (V) is satisfied.

It is important to take measures against heat generation from the EL display panel. As a measure against heat generation, a chassis 2062 made of metal material is mounted on the back of the panel (the side opposite to the illuminating surface of the display screen 50) as illustrated in Figure 206. For better heat dissipation, the chassis 2062 is provided with projections and depressions 2063. Also, a bonding layer is placed between the chassis 2061 and panel (the sealing lid 85 in the case of Figure 206). A material with good thermal conductivity is used for the bonding layer. Possible materials include, for example, silicone-resin paste and silicone paste. These materials are often used as an adhesive between a regulator IC and radiator plate. Incidentally, it is not strictly necessary for the bonding layer to have a bonding function as long as it serves the function of keeping the chassis 2061 and panel in intimate contact with each other.

Holes 2071 are provided in the back surface of the chassis 2062 as illustrated in Figure 207(a). The holes 2071 are

provided to release excess resin when the chassis 2062 and panel are bonded together. Also, the shape of the holes is varied between the center and periphery of the panel as shown in Figure 207(a) to adjust thermal resistance of the chassis 2062, and thereby make the panel temperature uniform. In Figure 207(a), the holes 2071c in the periphery of the panel are made larger than the holes 2071a in the center of the panel, thereby increasing the thermal resistance on the periphery of the panel. Consequently, the periphery of the panel is less liable to heat loss. This allows uniform heat distribution over the entire panel surface. Incidentally, the holes 2071 may be circular or the like as illustrated in Figure 207(b).

Figure 208 illustrates a configuration of the display panel according to the present invention. A flexible board 84 is mounted on one side of the array board 71. A power supply circuit 82 and the flexible board 84 are placed on the flexible board. Figure 209 shows a sectional view taken along line A-A' in Figure 208. However, in Figure 209, the flexible board 84 has been bent and the chassis 2062 has been mounted. As can be seen from Figure 209, the transformer 2011 of the power supply circuit 82 is contained in a space provided in the sealing lid 85. This makes it possible to reduce the thickness of the EL display panel (EL display panel module).

Next, description will be given of examples of display devices according to the present invention which run the drive systems according to the present invention. Figure 57 is a plan view of a cell phone which is an example of an information terminal. An antenna 571, numeric keys 572, etc. are mounted on a casing 573. Reference numerals 572 and the like denote a display color switch key, power key, and frame rate switch key.

The numeric key 572 may be configured to switch among color modes as follows: pressing it once enters 8-color display mode, pressing it again enters 4096-color display mode, and pressing it again enters 260,000-color display mode. The key is a toggle switch which switch among color display modes each time it is pressed. Incidentally, a display color change key may be provided separately. In that case, three (or more) numeric keys 572 are needed.

In addition to a push switch, the numeric key 572 may be a slide switch or other mechanical switch. Speech recognition may also be used for switching. For example, the switch may be configured such that display colors on the display screen 50 of the display panel will change as the user speaks a phrase such as "high-definition display," "4096-color mode," or "low-color display mode" into the phone. This can be implemented easily using existing speech recognition technology.

Also, display colors may be switched electrically. It is also possible to employ a touch panel which allows the user to make a selection by touching a menu presented on the display part 21 of the display panel. Besides, display colors may be switched based on the number of times the switch is pressed or based on a rotation or direction as is the case with a click ball.

A key which changes frame rate or a key which switches between moving pictures and still pictures many be used in place of the display color switch key 572. A key may switch two or more items at the same time: for example, among frame rates and between moving pictures and still pictures. Also, the key may be configured to change the frame rate gradually (continuously) when pressed and held. For that, among a capacitor C and a resistor R of an oscillator, the resistor R can be made variable or replaced with an electronic regulator. Alternatively, a trimmer capacitor may be used as a capacitor C of the oscillator. Such a key can also be implemented by forming a plurality of capacitors in a semiconductor chip, selecting one or more capacitors, and connecting the capacitors in parallel.

Furthermore, embodiments which use the EL display panel, EL display apparatus, or drive method according to the present invention will be described with reference to drawings.

Figure 58 is a sectional view of a viewfinder according to an embodiment of the present invention. It is illustrated schematically for ease of explanation. Besides, some parts are enlarged, reduced, or omitted. For example, an eyepiece cover is omitted in Figure 58. The above items also apply to other drawings.

Inner surfaces of a casing 573 are dark- or black-colored. This is to prevent stray light emitted from an EL display panel (EL display apparatus) 574 from being reflected diffusely inside the casing 573 and lowering display contrast. A phase plate ($\lambda/4$) 108, polarizing plate 109, and the like are placed on an exit side of the display panel. This has also been described with reference to Figures 10 and 11.

An eye ring 581 is fitted with a magnifying lens 582. The observer focuses on a display image 50 on the display panel 574 by adjusting the position of the eye ring 581 in the casing 573.

If a convex lens 583 is placed on the exit side of the display panel 574 as required, principal rays entering the magnifying lens 582 can be made to converge. This makes it possible to reduce the diameter of the magnifying lens 1582, and thus reduce the size of the viewfinder.

Figure 59 is a perspective view of a video camera. A video camera has a taking (imaging) lens 592 and a video camera casing 573. The taking lens 592 and the casing (viewfinder)

573 are mounted back to back with each other. The viewfinder 573 (see also Figure 58) is equipped with an eyepiece cover. The observer views the image 50 on the display panel 574 through the eyepiece cover.

The EL display panel according to the present invention is also used as a display monitor. The display screen 50 can pivot freely on a point of support 591. The display screen 50 is stored in a storage compartment 593 when not in use.

A switch 594 is a changeover switch or control switch and performs the following functions. The switch 594 is a display mode changeover switch. The switch 594 is also suitable for cell phones and the like. Now the display mode changeover switch 594 will be described.

The drive methods according to the present invention include the one that passes an N times larger current through EL elements 15 to illuminate them for a period equal to 1/M of 1F. By varying this illumination period, it is possible to change brightness digitally. For example, designating that N = 4, a four times larger current is passed through the EL elements 15. If the illumination period is 1/M, by switching M among 1, 2, 3, and 4, it is possible to vary brightness from 1 to 4 times. Incidentally, M may be switched among 1, 1.5, 2, 3, 4, 5, 6, and so on.

The switching operation described above is used for cell phones, which display the display screen 50 very brightly at

power-on and reduce display brightness after a certain period
to save power. It can also be used to allow the user to set
a desired brightness. For example, the brightness of the
screen is increased greatly outdoors. This is because the
screen cannot be seen at all outdoors due to bright surroundings.
However, the EL elements 15 deteriorate quickly under
conditions of continuous display at high brightness. Thus,
the screen 50 is designed to return to normal brightness in
a short period of time if it is displayed very brightly. A
button which can be pressed to increase display brightness
should be provided, in case the user wants to display the screen
50 at high brightness again.

Thus, it is preferable that the user can change display
brightness with the switch 594, that the display brightness
can be changed automatically according to mode settings, or
that the display brightness can be changed automatically by
detecting the brightness of extraneous light. Preferably,
display brightness settings such as 50%, 60%, 80%, etc. are
available to the user.

Preferably, the display screen 50 employs Gaussian
display. That is, the center of the display screen 50 is bright
and the perimeter is relatively dark. Visually, if the center
is bright, the display screen 50 seems to be bright even if
the perimeter is dark. According to subjective evaluation,
as long as the perimeter is at least 70% as bright as the center,

there is not much difference. Even if the brightness of the
perimeter is reduced to 50%, there is almost no problem. The
self-luminous display panel according to the present invention
generates a Gaussian distribution from top to bottom of the
screen using the N-fold pulse driving described above (a method
which passes an N times larger current through EL elements
15 to illuminate them for a period equal to 1/M of 1F).

Specifically, the value of M is increased in upper and
lower parts of the screen and decreased in the center of the
screen. This is accomplished by modulating the operating
speed of a shift register of the gate driver circuits 12. The
brightness at the left and right of the screen is modulated
by multiplying video data by table data. By reducing
peripheral brightness (at an angle of view of 0.9) to 50% through
the above operation, it is possible to reduce power consumption
by 20% compared to brightness of 100%. By reducing peripheral
brightness (at an angle of view of 0.9) to 70%, it is possible
to reduce power consumption by 15% compared to brightness of
100%.

Preferably a changeover switch is provided to enable and
disable the Gaussian display. This is because the perimeter
of the screen cannot be seen at all outdoors if the Gaussian
display is used. Thus, it is preferable that the user can
change display brightness with the button switch, that the
display brightness can be changed automatically according to

mode settings, or that the display brightness can be changed automatically by detecting the brightness of extraneous light. Preferably, display brightness settings such as 50%, 60%, 80%, etc. are available to the user.

Liquid crystal display panels generate a fixed Gaussian distribution using a backlight. Thus, they cannot enable and disable the Gaussian distribution. The capability to enable and disable Gaussian distribution is peculiar to self-luminous display devices.

A fixed frame rate may cause interference with illumination of an indoor fluorescent lamp or the like, resulting in flickering. Specifically, if the EL elements 15 operate on 60-Hz alternating current, a fluorescent lamp illuminating on 60-Hz alternating current may cause subtle interference, making it look as if the screen were flickering slowly. To avoid this situation, the frame rate can be changed. The present invention has a capability to change frame rates. Also, it allows the value of N or M to be changed in N-fold pulse driving (a method which passes an N times larger current through EL elements 15 to illuminate them for a period equal to 1/M of 1F).

The above capabilities are implemented by way of the switch 594. The switch 594 switches among the above capabilities when pressed more than once, following a menu on the screen 50.

Incidentally, the above items are not limited to cell phones. Needless to say, they are applicable to television sets, monitors, etc. Also, it is preferable to provide icons on the display screen to allow the user to know at a glance what display mode he/she is in. The above items similarly apply to the following.

The EL display apparatus and the like according to this embodiment can be applied not only to video cameras, but also to digital cameras such as the one shown in Figure 60, still cameras, etc. The display apparatus is used as a screen 50 attached to a camera body 601. The camera body 601 is equipped with a switch 594 as well as a shutter 603.

The display panel described above has a relatively small display area. However, with a display area of 30 inches or larger, the display screen 50 tends to flex. To deal with this situation, the present invention puts the display panel in a frame 611 and attaches a fitting 614 so that the frame 611 can be suspended as shown in Figure 61. The display panel is mounted on a wall or the like using the fitting 614.

A large screen size increases the weight of the display panel. As a measure against this situation, the display panel is mounted on a stand 613, to which a plurality of legs 612 are attached to support the weight of the display panel.

The legs 612 can be moved from side to side as indicated by A. Also, they can be contracted as indicated by B. Thus, the display apparatus can be installed even in a small space.

A television set in Figure 61 has a surface of its screen covered with a protective film (or a protective plate). One purpose of the protective film is to prevent the surface of the display panel from breakage by protecting from being hit by something. An AIR coat is formed on the surface of the protective film. Also, the surface is embossed to reduce glare caused by extraneous light on the display panel.

A space is formed between the protective film and display panel by spraying beads or the like. Fine projections are formed on the rear face of the protective film to maintain the space between the protective film and display panel. The space prevents impacts from being transmitted from the protective film to the display panel.

Also, it is useful to inject an optical coupling agent into the space between the protective film and display panel. The optical coupling agent may be a liquid such as alcohol or ethylene glycol, a gel such as acrylic resin, or a solid resin such as epoxy. The optical coupling agent can prevent interfacial reflection and function as a cushioning material.

The protective film may be, for example, a polycarbonate film (plate), polypropylene film (plate), acrylic film (plate), polyester film (plate), PVA film (plate), etc. Besides, it

goes without saying that an engineering resin film (ABS, etc.) may be used. Also, it may be made of an inorganic material such as tempered glass. Instead of using a protective film, the surface of the display panel may be coated with epoxy resin, phenolic resin, and acrylic resin 0.5 mm to 2.0 mm thick (both inclusive) to produce a similar effect. Also, it is useful to emboss surfaces of the resin.

It is also useful to coat surfaces of the protective film or coating material with fluorine. This will make it easy to wipe dirt from the surfaces with a detergent. Also, the protective film may be made thick and used for a front light as well as for the screen surface.

The display panel according to the example of the present invention may be used in combination with the three-side free configuration. The three-side free configuration is useful especially when pixels are built using amorphous silicon technology. Also, in the case of panels formed using amorphous silicon technology, since it is difficult to control variations in the characteristics of transistor elements during production processes, it is preferable to use the N-pulse driving, reset driving, dummy pixel driving, or the like according to the present invention. That is, the transistors according to the present invention are not limited to those produced by polysilicon technology, and they may be produced by amorphous silicon technology.

Incidentally, the N-fold pulse driving (Figures, 13, 16, 19, 20, 22, 24, 30, etc.) and the like according to the present invention are more effective for display panels which contain transistors 11 formed by low-temperature polysilicon technology than display panels which contain transistors 11 formed by amorphous silicon technology. This is because adjacent transistors, when formed by amorphous silicon technology, have almost equal characteristics. Thus, driving currents for individual transistors are close to a target value even if the transistors are driven by current obtained by addition (the N-fold pulse driving in Figures 22, 24, and 30, in particular, are effective for pixel configurations containing amorphous silicon transistors).

The duty cycle control driving, reference current control, N-fold pulse driving, and other drive methods and drive circuits according to the present invention described herein are not limited to drive methods and drive circuits for organic EL display panels. Needless to say they are also applicable to other displays such as field emission displays (FEDS) as shown in Figure 221.

In an FED shown in Figure 221, an electron emission protuberance 2213 (which corresponds to the pixel electrode 105 in Figure 10) which emits electrons in a matrix is formed on a board 71. A pixel contains a holding circuit 2214 (which corresponds to the capacitor in Figure 1) which holds image

data received from a video signal circuit 2212 (which corresponds to the source driver circuit 14 in Figure 1). Also, control electrodes 2211 are placed in front of the electron emission protuberance 2213. Voltage signals are applied to the control electrodes 2211 by an on/off control circuit 2215 (which corresponds to the gate driver circuit 12 in Figure 1).

The pixel configuration in Figure 221 can perform N-fold pulse driving, duty cycle control driving, etc. if a peripheral circuit shown in Figure 222 is added. An image data signal is applied to the source signal line 18 from the video signal circuit 2212. A pixel 16 selection signal is applied to a selection signal line 2221 by an on/off control circuit 2215a, and consequently pixels 16 are selected one after another and image data is written into them. Also, an on/off signal is applied to an on/off signal line 2222 by an on/off control circuit 2215b, and consequently the FED of pixels is subjected to on/off control (duty cycle control).

The technical idea described in the example of the present invention can be applied to video cameras, projectors, 3D television sets, projection television sets, etc. It can also be applied to viewfinders, cell phone monitors, PHS, personal digital assistants and their monitors, and digital cameras and their monitors.

Also, the technical idea is applicable to electrophotographic systems, head-mounted displays, direct view monitors, notebook personal computers, video cameras, electronic still cameras. Also, it is applicable to ATM monitors, public phones, videophones, personal computers, and wristwatches and its displays.

Furthermore, it goes without saying that the technical idea can be applied to display monitors of household appliances, pocket game machines and their monitors, backlights for display panels, or illuminating devices for home or commercial use. Preferably, illuminating devices are configured such that color temperature can be varied. Color temperature can be changed by forming RGB pixels in stripes or in dot matrix and adjusting currents passed through them. Also, the technical idea can be applied to display apparatus for advertisements or posters, RGB traffic lights, alarm lights, etc.

Also, organic EL display panels are useful as light sources for scanners. An image is read with light directed to an object using an RGB dot matrix as a light source. Needless to say, the light may be monochromatic. Besides, the matrix is not limited to an active matrix and may be a simple matrix. The use of adjustable color temperature will improve imaging accuracy.

Also, organic EL display panels are useful as backlights of liquid crystal display panels. Color temperature can be

changed and brightness can be adjusted easily by forming RGB pixels of an EL display panel (backlight) in stripes or in dot matrix and adjusting currents passed through them. Besides, the organic EL display panel, which provides a surface light source, makes it easy to generate Gaussian distribution that makes the center of the screen brighter and perimeter of the screen darker. Also, organic EL display panels are useful as backlights of field-sequential liquid crystal display panels which scan with R, G, and B lights in turns. Also, they can be used as backlights of liquid crystal display panels for movie display by inserting black even if the backlights are turned on and off.

Industrial Applicability

The source driver circuit of the present invention, in which transistors composing a current mirror are formed adjacent to each other, can reduce variations in output current caused by deviations in thresholds. Thus, it can reduce brightness irregularities of an EL display panel and has great practical effect.

Also, the display panels, display apparatus, etc. of the present invention offer distinctive effects, including high quality, high movie display performance, low power consumption, low costs, high brightness, etc., according to their respective configurations.

Incidentally, the present invention does not consume much power because it can provide power-saving information display apparatus. Also, it does not waste resources because it can reduce size and weight. Furthermore, it can adequately support high-resolution display panels. Thus, the present invention is friendly to both global environmental and space environment.